Spring 6-11-2015

Improved Gain Stability of a Digital Imager Using a Charge Feedback Amplifier

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by

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A thesis submitted in partial fulfillment of the
requirements for the degree of

Master of Science
in
Physics

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Portland State University
2015

Abstract

Digital imagers including Charge-Coupled Devices (CCD) are essential to most forms of modern photographic technologies. The quality of the data produced by digital imagers have made them an invaluable scientific measurement tool. Despite the numerous advantages of digital imagers, there are still factors that limit their performance. One such factor is the stability of the camera's gain, the ratio that dictates the imager's ability to convert incident photons to a measurable output voltage. Variations in gain can affect the linearity of the device and produce inaccurate measurements.

One of the factors that determines the gain of the camera is the sensitivity of the output amplifier. The purpose of this study is to compare the performance of two different output amplifier structures: the traditional source follower (SF) and the charge feedback amplifier (CFA). In studies of other solid state detectors, the CFA has shown a greater stability against variations in certain system parameters and environmental conditions such as operating temperature. It is thought that the CFA shows a superior stability over the SF, because the gain of the SF is dependent on multiple capacitances associated with the reset and output transistors, whereas the CFA gain is only dependent on its feedback capacitance. Furthermore, the CFA is able to handle a larger amount of charge than the SF, which increases the dynamic range of the output amplifier.

In this research, output amplifier stability is measured using gain and linearity data collected from a CCD manufactured with both types of amplifiers. Preliminary data is presented that indicates the CFA exhibits a greater linearity, larger dynamic range, and a more stable gain than the SF. Despite this the CFA suffers from a significantly larger level of noise. Suggestions for future research are also given.

Acknowledgements

I would like to thank Dr. Barry Burke and Daniel O'Mara for giving us this project and for their continued technical support and advice throughout this study.

Thank you to Dr. Morley Blouke for sharing so much of his expertise and vast experience in digital imagers. It has been an honor to have worked with such an important figure in CCD research.

Marc Nisenfeld and Alex Chally from the university machine shop provided invaluable assistance in building some of the equipment vital to this project and then repairing the components once I broke them. Leroy Laush from the university electronics shop greatly improved the circuitry used in this study and elucidated so many aspects of the camera electronics. Without their support, I would still be struggling to record my first data set.

Thank you to my sisters Grace Weatherford and Liz Moorehead and my father Jim Mylott, who have all been ceaselessly supportive and encouraging.

Finally, I would like to thank Dr. Erik Bodegom and Dr. Ralf Widenhorn who had the confidence in me to invite me into their lab and join in their research. Their support and guidance in all things scientific, academic, and administrative have been thoroughly enriching.

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1.0 Introduction and Background Information

Digital imaging sensors have become essential to most every form of commercial and scientific photography. They can be found in virtually every kind of photographic device including cell phones, laptops, microscopes, telescopes, and satellites. They are also widely used in many non-photographic systems such as spectrometers. Analog imaging technology can not compete with digital imagers' size, performance, or cost.

Despite the superior performance and versatility of digital imagers, there are still a number of factors that limit their performance including the camera gain. The gain of a camera is a conversion factor that measures the ability of a Charge-Coupled Device (CCD) to convert an absorbed photon into an output voltage. Variations in gain can affect the linearity of the device and produce inaccurate measurements. One of the factors that determine the gain of the camera is the sensitivity of the output amplifier. Improving the stability of the amplifier sensitivity will also improve the camera stability. Among the most prevalent output amplifier architectures is the source follower (SF), which is comprised of at least two MOSFETs. Another method of converting charge to a voltage is the charge feedback amplifier (CFA). CFAs are used extensively in other detection equipment such as scintillation counters, but have not been widely used in digital imagers. The stability of CFAs could potentially make them a desirable alternative to traditional amplifiers for digital imaging.

The purpose of this study is to compare the performance of a traditional SF output

amplifier to the CFA. Specifically, the noise of both amplifiers will be compared as well as their gain stability and linearity. The stability of both amplifiers as a function of temperature will also be explored. In order to conduct these experiments, a camera system had to be developed. Additionally, original software was created to operate the camera and to collect and analyze data. All of these components, as well as the data collected, will be discussed.

1.1 Charge Coupled Devices

The CCD is one of the most common types of digital imager. It was invented at Bell Laboratories by Willard S. Boyle and George E. Smith in 1969, for which they would win the Nobel prize in physics in 2009. CCDs have been used in astronomy since 1976 and have been available in consumer cameras since the early 1980s. Many satellite observatories have utilized CCDs as their primary imaging methodology including the Hubble and Kepler telescopes. The imager used in this experiment is a CCD manufactured at Lincoln Laboratories in Massachusetts and will be described in a later section. What follows in this chapter is a description of the structure and function of a CCD.

1.2 Charge Generation, Storage, and Transfer

A CCD is comprised of an array of closely spaced metal-oxide-semiconductor (MOS) capacitors. The MOS capacitor itself is composed of a doped silicon substrate and a metal gate electrode separated by an oxide layer (Fig. 1.1). A positive gate voltage (V_G) that is greater than the flat-band voltage (V_{FB}) but less than the threshold voltage (V_T) will create a region under the oxide layer depleted of the majority carriers

(holes in the case of p-type semiconductors), which are repelled by the positive charges on the gate. The only charges left in the depletion region are the negatively charged ions in the substrate (Fig. 1.2). Under these conditions, the MOS capacitor is in the so called depletion mode. By increasing the gate voltage above the threshold voltage, the capacitor transitions into the inversion mode. The increase in positive charges on the gate attracts minority carriers (electrons), which form an inversion layer. The inversion layer is the potential well of the CCD and has a charge capacity given by $Q_{n,sat} = C_{OX} \cdot (V_G - V_T)$, where C_{OX} is the capacitance of the oxide layer [17].

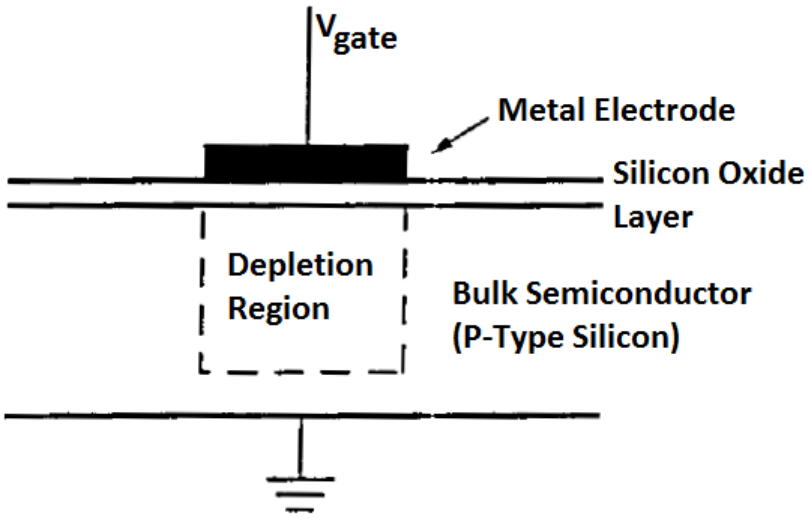


Figure 1.1: The structure of a MOS capacitor. [8].

If an incident photon that interacts with the substrate of the MOS capacitor has an energy greater than the band gap of the substrate, an electron will be promoted from the valence band to the conduction band, creating an electron-hole pair. If the electric field created by the gate electrode is sufficiently large, the MOS capacitor will be in the inversion mode as described above. The e-h pairs will separate so that minority carriers (electrons) will collect inside the inversion layer and majority carriers (holes) will be repelled into the substrate. Photon energies between 1.1 to 3.1

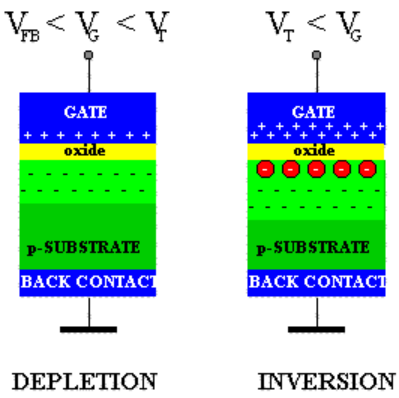


Figure 1.2: Raising the gate voltage causes the capacitor to go into the inversion mode, which creates an inversion layer of charge [18].

eV will produce a single electron-hole pair per photon, thus the number of minority carriers in the potential well should be proportional to the number of interacting photons with wavelengths of approximately 400-1100 nm [9].

The accumulated charge in the potential well is shifted by manipulating the potential on the gate electrode of a neighboring MOS capacitor. The charge transfer in a three phase CCD is depicted in Fig. 1.3. In the first phase, every third MOS capacitor has a gate voltage that creates a potential well where electrons can be collected. In phase two, the gate voltage of the neighboring capacitor is raised to the same potential as the original capacitor, doubling the size of the well. Charge spreads evenly through the combined inversion layer of both capacitors. Finally, in phase three, the gate voltage of the original capacitor is lowered, removing its potential well. The charge is now held by the second capacitor. Electrons are moved to the third capacitor in the same way. Thus, in a three phase device, a single pixel of the resulting image is made up of three MOS capacitors. Charge is moved through these parallel gates to the serial register at the bottom of the chip. The serial register is made up of MOS capacitors as well and shifts charge into the charge to voltage converter in a similar fashion (Fig. 1.4).

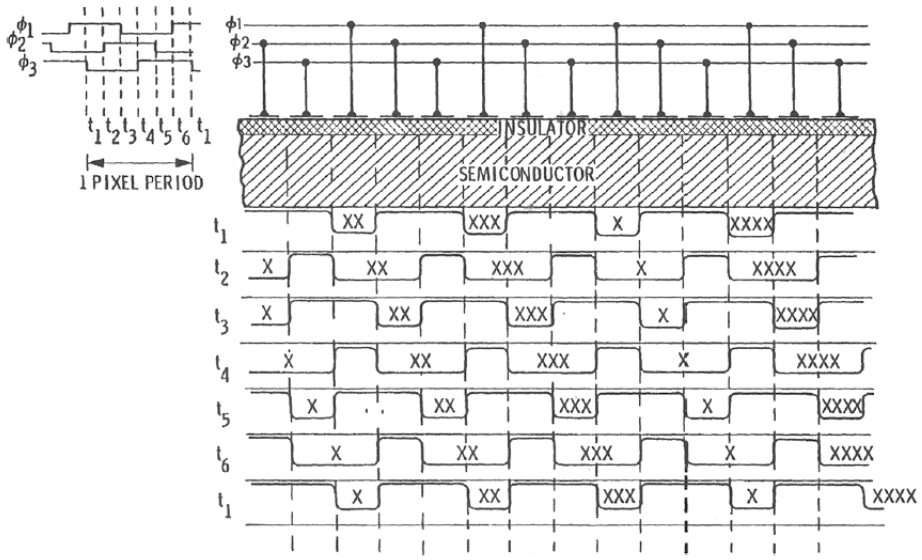


Figure 1.3: Charge can be transferred through the parallel MOS capacitors by changing the gate voltages of neighboring capacitors [9].

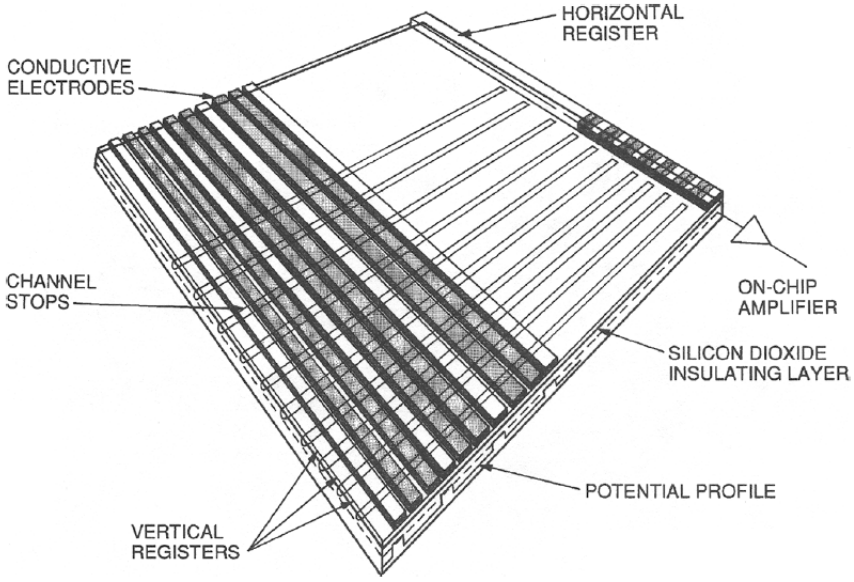


Figure 1.4: The collected charge is moved through the parallel or vertical registers as described in Fig. 1.3. At the bottom of the array, charge moves from the parallel wells to the serial or horizontal wells and read out individually [9].

1.3 Charge Measurement

After the charge is shifted from the parallel gates to the serial register, it is moved past the output transfer gate (OTG) into the sense node (Fig. 1.5). The OTG is held at a DC potential and serves as a buffer between the final serial gate and the sense node. The sense node is connected to the source of the reset transistor. Charge at the sense node is measured using a method called correlated double sampling (CDS). In this method, charge in the sense node is cleared by pulsing the potential on the reset gate and the sense node is measured. Next the charge in the final phase of the serial register is shifted past the OTG and into the sense node. The extra electrons decrease the potential of the sense node, which is measured again. The signal in that pixel is the difference between the two sense node measurements. The reset and output waveforms are illustrated in Fig. 1.6.

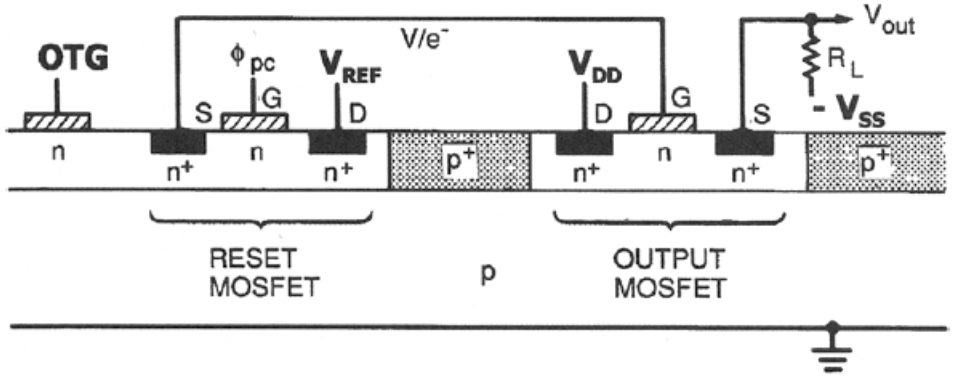


Figure 1.5: The output structure of a CCD. Charge from the serial register is clocked past the OTG into the sense node, which is connected to the source of the reset transistor [9].

The method by which the charge in the sense node is measured is the purpose of this experiment. Specifically two methods will be compared: the traditional source follower (SF) and the charge feedback amplifier (CFA).

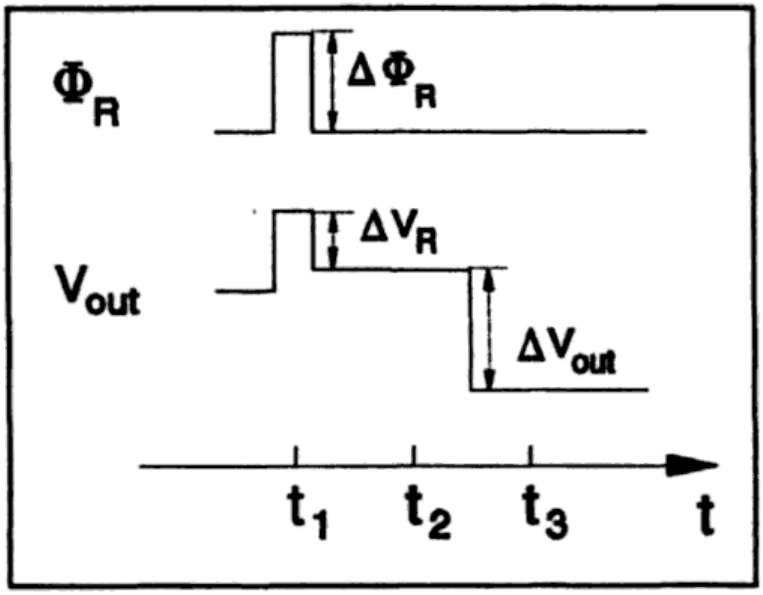


Figure 1.6: The output timing diagram of correlated double sampling. At t_1 the reset gate is pulsed, clearing the charge from the sense node. At time t_2 the potential of the sense node decreases from the reset level to the reference level. At time t_3 the charge in the final serial gate is clocked into the sense node, decreasing the potential. The signal in the pixel is proportional to the difference in potentials measured at time t_2 and t_3 [17].

Source Follower

The most common method of measuring the potential of the sense node is to use a source follower, in which the source of the reset transistor is connected to the gate of a second transistor (Fig. 1.7). The drain of the output transistor is held at a constant potential V_{DD}. As the sense node voltage changes due to an increase in charge, the gate of the output transistor varies the amount of current through the output transistor. This is measured as a change in the voltage at the source of the second transistor across a load R_L.

Sensitivity is a measure of the output amplifier to convert charge to voltage, and is given by the equation

$$S_{SF} = \frac{q}{C_S}, \tag{1.1}$$

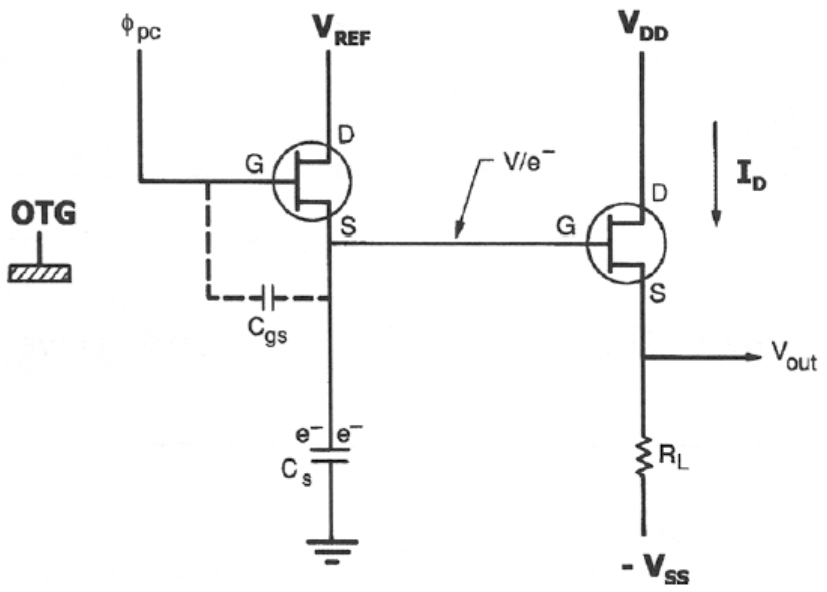


Figure 1.7: The output circuit diagram of the source follower method of measuring the charge in the sense node of the reset transistor [9].

where S_{SF} is the sensitivity in units of volts per electron, C_S is the sense capacitance in farads, and q is the elemental charge [9, 12]. The sense capacitance is dependent on the capacitances associated with both the output and reset transistors and is given by [9]

$$C_S = C_{FD} + C_{MOS} = C_{FD} + C_{GS} + C_{GD} + C_G, \tag{1.2}$$

where C_{FD} is the capacitance associated with the floating diffusion, C_{MOS} is the gate capacitance of the output MOSFET, and C_{GS}, C_{GD}, and C_G are the gate to source, gate to drain, and gate area capacitances of the output MOSFET respectively. Thus, any fluctuations in the capcitances of the output transistor will result in a nonlinear output amplifier sensitivity.

Charge Feedback Amplifier

Figure 1.8 represents a typical CFA. The CFA is a charge to voltage converter like the SF, but has a sensitivity proportional to only one capacitor. No charge is stored in the sense node, because the feedback loop keeps the sense node at a virtual ground. All the charge collected by the detector is integrated onto the feedback capacitor. This creates an output voltage opposite in polarity to the input voltage and inversely proportional to the capacitance in the feedback loop [1, 7, 15]. Two assumptions are made when considering an ideal CFA:

1. The input of the amplifier draws zero current.
2. The open loop gain of the amplifier is infinite.

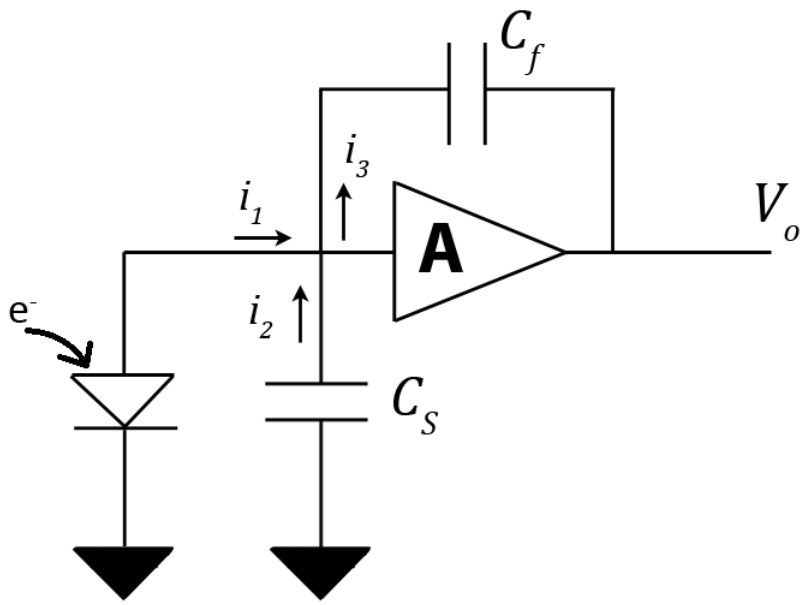


Figure 1.8: An example of a charge feedback amplifier circuit.

The gain of the CFA is given by

$$V_o = -AV_i. \tag{1.3}$$

The voltage across the capacitor is

$$V_c = V_o - V_i = V_o + \frac{V_o}{A} = V_o\Big(1 + \frac{1}{A}\Big) \tag{1.4}$$

The sensitivity of the CFA can be found by applying Kirchoff's Current Law (KCL). KCL states that the sum of currents entering a node is equal to the sum of the currents leaving the node. Because the amplifier has zero input current,

$$i_1 + i_2 + i_3 = 0, \tag{1.5}$$

where i_1 is the current collected by the detector, i_2 is the current through the sense node capacitor, and i_3 is the current through the feedback capacitor. i_1 is simply the rate at which charge is deposited into the sense node. i_2 and i_3 are found using equation for the current through a capacitor.

$$i_1 = \frac{\mathrm{d}Q}{\mathrm{d}t} \tag{1.6}$$

$$i_2 = -C_s\frac{\mathrm{d}V_i}{\mathrm{d}t} = \frac{C_s}{A}\frac{\mathrm{d}V_o}{\mathrm{d}t} \tag{1.7}$$

$$i_3 = C_f\frac{\mathrm{d}V_c}{\mathrm{d}t} = C_f\Big(1 + \frac{1}{A}\Big)\frac{\mathrm{d}V_o}{\mathrm{d}t} \tag{1.8}$$

Inserting these into 1.5 gives

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = -\frac{\mathrm{d}V_o}{\mathrm{d}t}\Big(\frac{C_s}{A} + C_f\Big(1 + \frac{1}{A}\Big)\Big). \tag{1.9}$$

Integrating results in

$$\frac{V_o}{Q} = -\Big(\frac{C_s}{A} + C_f\Big(1 + \frac{1}{A}\Big)\Big)^{-1}. \tag{1.10}$$

If the gain of the amplifier is infinite, this reduces to

$$\frac{V_o}{Q} = -\frac{1}{C_f}. \tag{1.11}$$

The amplitude of the signal is given by

$$Q = \eta_i \cdot q, \tag{1.12}$$

where η_i is the number of electron-hole pairs generated by a photon and q is the elemental charge. Therefore the sensitivity of the CFA is

$$S_{CFA} = \frac{V_o}{\eta_i} = -\frac{q}{C_f}. \tag{1.13}$$

Eq. 1.1 states that the sensitivity of the SF is a function of multiple capacitances, but Eq. 1.13 shows that the sensitivity of the CFA is only dependent on the feedback capacitor. If that capacitor is stable, the gain and linearity of the CFA will not be subject to the variations in sensitivity that limit the SF output.

1.4 Camera Gain

The voltage created by the output amplifier is passed through a signal processing circuit and finally measured by an Analog to Digital Converter (ADC). The process of converting an incident photon to a Digital Number (DN) is depicted in Fig. 1.9.

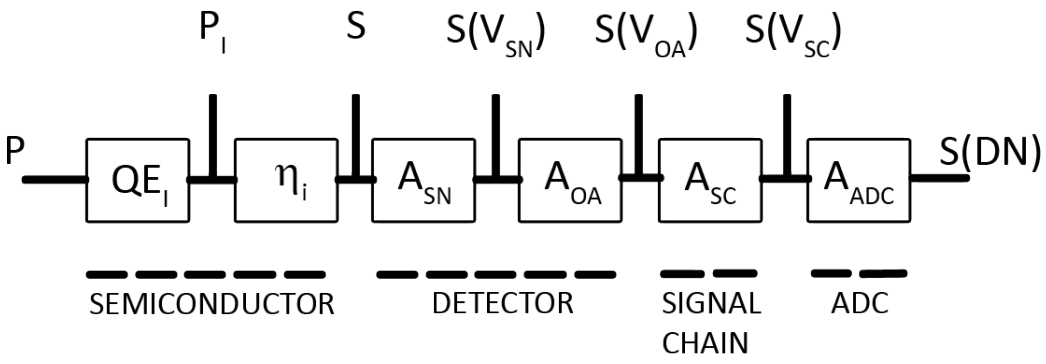


Figure 1.9: CCD block diagram showing the conversions starting with incident photons and ending with Digital Numbers. (Modified from [10]).

At each block in the diagram, there is a conversion from one unit to another. Each conversion has an associated gain. The gain of the camera A_{CCD} is simply the product of each of these gains and is given by [10]

$$A_{CCD} = QE_I \eta_i A_{SN} A_{OA} A_{SC} A_{ADC}. \tag{1.14}$$

Each parameter of Eq. 1.14 is listed in Table. 1.1. QE_I and η_i determine the number of electrons generated per incident photon. The gain of the output amplifier A_{OA} is a function of the amplifier's sensitivity.

Symbol	Description	Unit
A_{CCD}	camera gain	(DN/photon)
QE_I	interacting quantum efficiency	(photon/photon)
η_i	quantum yield	(e^-/photon)
A_{SN}	sense node gain	(V/e^-)
A_{OA}	on-chip amplifier gain	(V/V)
A_{SC}	signal chain gain	(V/V)
A_{ADC}	ADC gain	(DN/V)

Table 1.1: Summary of the gains depicted in Fig. 1.9 and Eq. 1.14.

This study utilizes a CCD that is fitted with both a SF and a CFA output, which will be described in a later section. Because both outputs are on the same chip and are being measured with the same ADC, the only variations between the measurements are due to the gains of the sense node, output amplifier, and the signal processing circuit. Equation 1.14 can be rewritten to isolate only these gains.

$$K = \frac{A_{CCD}}{QE_I\eta_i A_{ADC}} = A_{SN}A_{OA}A_{SC}, \tag{1.15}$$

where K is the gain of the camera in (V/e^-). The relative stability of the SF and CFA amplifiers are compared in this study using measurements of K. The following section will describe the effect variations in K have on the output signal as well as the methods used to measure K.

2.0 Experiment Design

As stated in the introduction, the CFA was proposed for its potential to increase the maximum output signal of the CCD as well as improve gain and linearity. This study was divided into two experiments: linearity and gain.

2.1 Linearity

The purpose of this experiment was to measure the maximum signal of the CFA and the SF outputs as well as the linearity of their response in the dynamic range. Linearity data can be represented in a linear transfer curve, which is simply a plot of the CCD output versus the exposure level. In this experiment, the exposure source was an array of LEDs in a light box, which will be described in a later section. The output of the CCD is a function of the LED flash count and is given by

$$S = fK + S_D, \tag{2.1}$$

where S is the signal in DN, f is the flash count of the LEDs, K is the gain of the CCD in DN/flash and S_D is the dark signal in DN. The first frame taken in the linear transfer curve has a zero exposure and is therefore equal to S_D. This value can be subtracted from each frame, so that S_D in Eq. 2.1 cancels out and the linear transfer curve intersects the origin. Figure 2.1(a) shows a preliminary linearity transfer curve

for the CFA of the CCID 22.5, which shows a gain of 183 DN/flash.

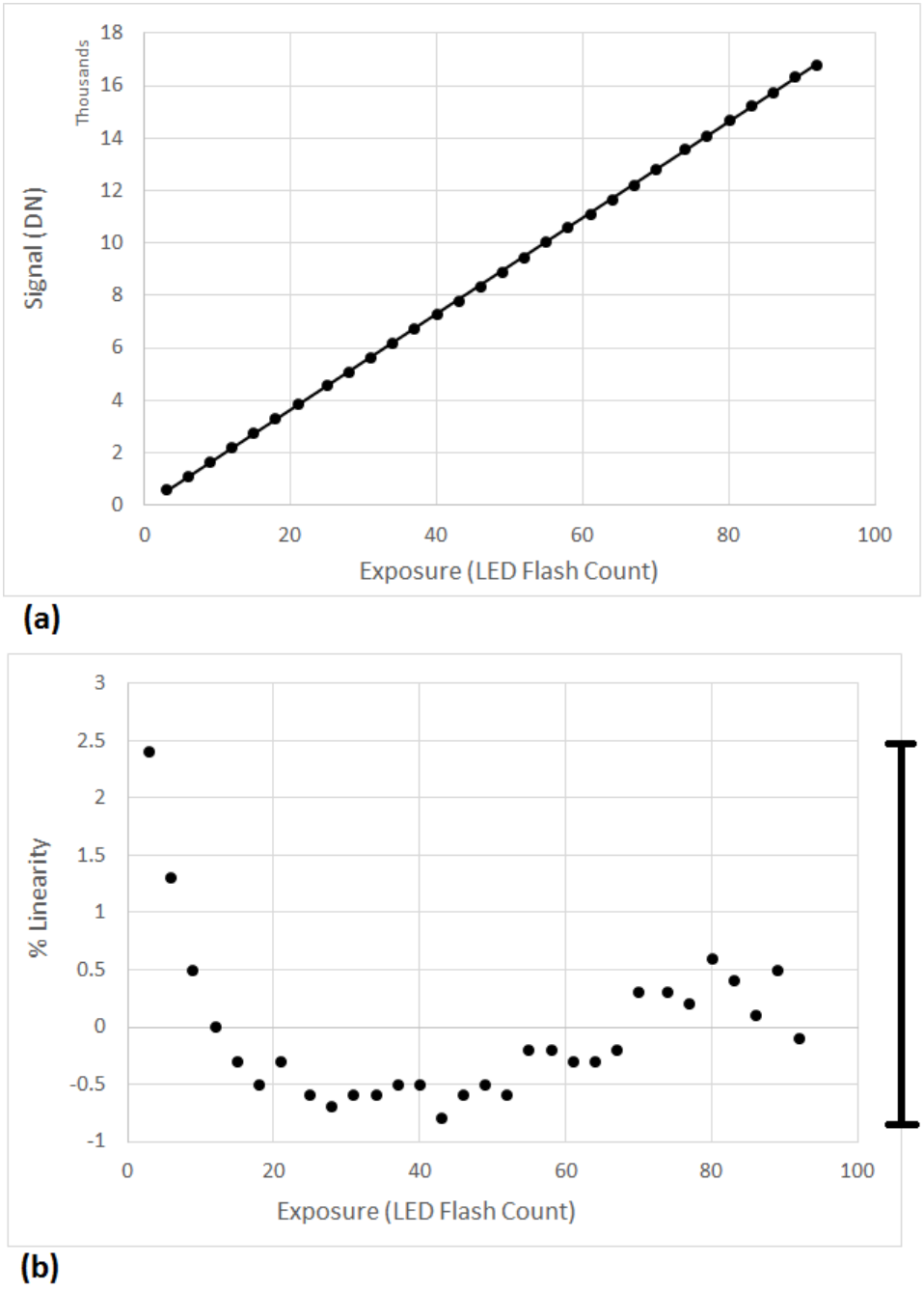


Figure 2.1: (a) Linearity transfer curve and (b) linearity residual curve for initial data taken with the CFA side of the CCID 22.5 digital imager, where $K = 183$ DN/flash and $\Delta LR = 3.2\%$

The linearity of data in the linear transfer curve can be measured using a quantity called the linear residual given by the equation

$$LR = 100\%\Big(1 - \frac{S_M/f_M}{S/f}\Big), \tag{2.2}$$

where LR is the linearity residual for a given LED flash count, S_M and f_M are the signal and LED flash count at half of the full well, and S and f are the signal and flash count of a given exposure. The LR of each data point in the linear transfer is calculated and plotted versus the LED flash count. The difference between the minimum and the maximum linearity residual ΔLR represents the linearity of the device [9]. For example, the data in Fig. 2.1 from the CCID 22.5 CFA side shows a 3.2% linearity over the dynamic range. This study is concerned with how the SF and CFA outputs respond to temperature changes, therefore linearity data was taken over the range -110 °C to 20 °C and ΔLR was plotted for each temperature.

The gain K acquired from the linear residual equation (Eq. 2.1) is given in the units DN/flash. The more common and useful unit for gain is $\mu V/e^-$, which can be found using the variance photon transfer curve (PTC) [10]. The variance PTC method uses the data collected for a linear transfer and is explained in the results section. It will also be shown in the results section that once the gain in $\mu V/e^-$ is known, the linear transfer curved can be converted from DN vs. flash count to the units of V versus e^-. The gain calculated by the PTC is a useful approximation, but lacks precision. The variation in gain versus temperature is small and requires a high precision measurement method. The next section details a method for measuring gain with higher precision.

2.2 Gain Stability

Sampietro et al. showed that gain as a function of temperature is more stable for a CFA than the traditional source follower amplifier due to variations in the MOSFET gate capacitance [15]. The experiment used in this study measures the variation in gain of the CFA and the SF outputs over a temperature range of -110 °C to 20 °C.

One of the most accurate methods to determine the gain of a CCD is the x-ray transfer. Visible photons have enough energy to create a single e-h pair in the silicon substrate of a CCD. X-ray photons have a much larger energy, which means that multiple e-h pairs will be produced in silicon by a single x-ray photon. FE^{55} is a source of 5.9 keV photons, which produce 1620±13 e^- when incident on a silicon substrate at room temperature [9]. The signal from the x-rays will show some variation due to a combination of noise sources. If enough events are recorded, the events will form a Gaussian distribution. The center of the Gaussian peak will be the average signal of the x-rays (Fig. 2.2).

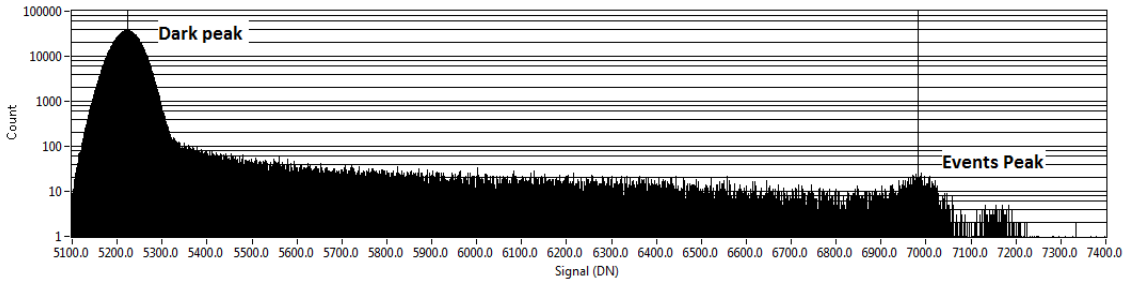


Figure 2.2: Histogram of the SF side of the CCID 22.5 made by combining 20 images.

The difference between the dark peak and the x-ray events peak represents the average number of electrons generated in each event and can be used to find the gain of the CCD using the equation

$$K = \frac{1620\mathrm{e}^{-}}{EventsPeak - DarkPeak}, \tag{2.3}$$

where K is the gain of the CCD in e^{-}/DN. The gain can also be expressed in μV/e^{-} by converting the peak measurements using the gain of the analog to digital converter or data acquisition unit (DAQ).

The histogram in Fig. 2.2 is a combination of multiple images, which is necessary to compute the gain because of split pixel events. The charges generated by the x-rays will be tightly clustered, approximately 0.4 µm in diameter [9]. This is much smaller than the 15 µm x 15 µm pixel dimension of the CCID 22.5, so most charge clouds will be captured within a single pixel. However, frequently clouds will form either on the boundary between pixels or below the depletion region and can diffuse into adjacent pixels [9]. This causes a split pixel event.

Figure 2.3(a) is an image taken from the CFA side of the CCID 22.5 when exposed to an FE^{55} source. The individual x-ray events can be seen in (b). There are three split pixel events, and two single pixel events. Rather than creating a single Gaussian peak, this has the effect of creating a tail to the right of the main peak in the image histogram (2.3(c)). For this reason, a single image was not sufficient to determine the location of the x-ray event peak and therefore the gain of the CCD.

The events peak can be made visible by combining multiple images. For example, the histogram in Fig. 2.2 was made using 20 images all taken at the same temperature and exposure conditions.

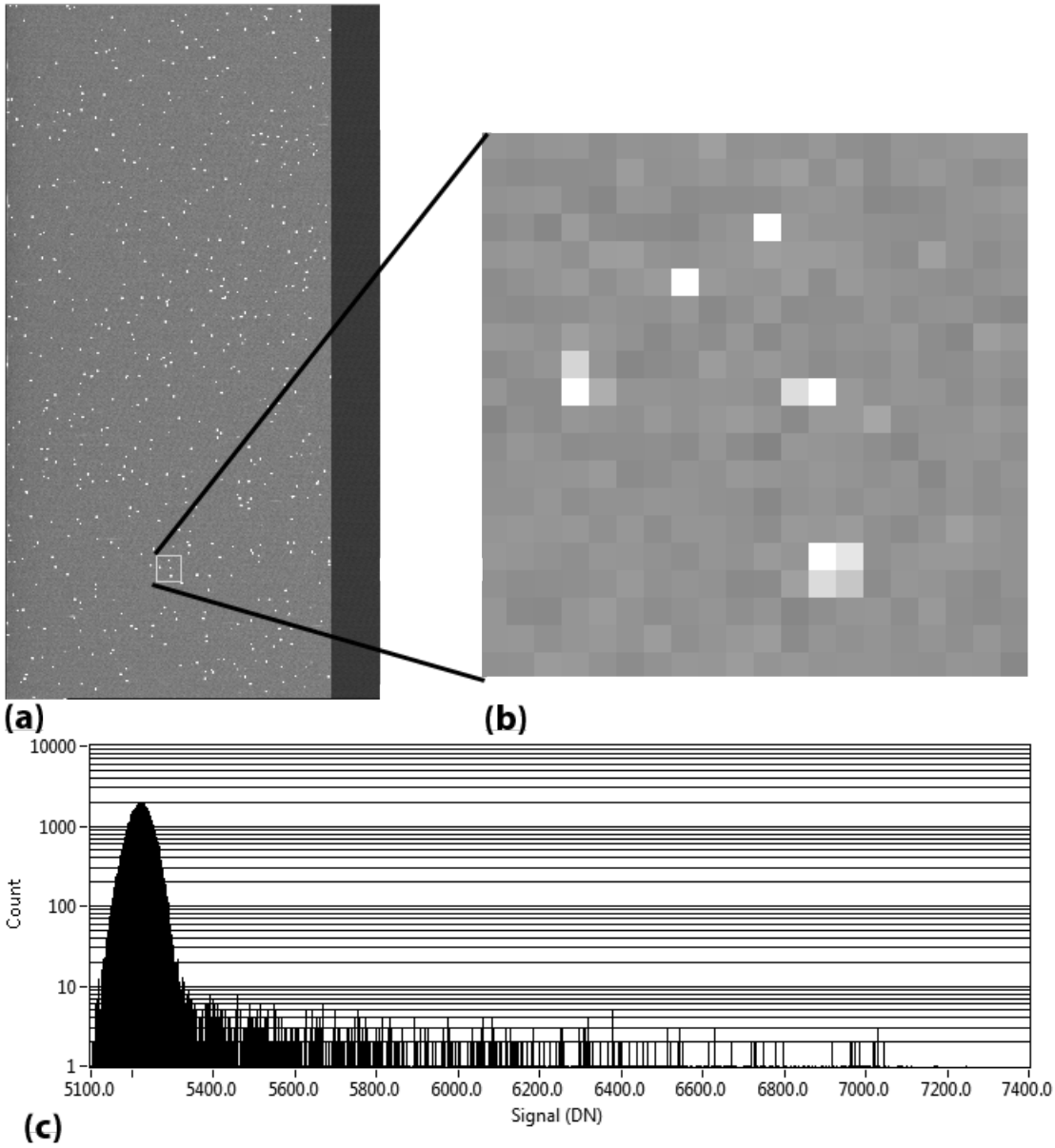


Figure 2.3: (a) Image from the SF side of the CCID 22.5 after being exposed to an FE^{55} source. (b) An elargement of the image in (a) showing both single and split pixel events. (c) Histogram of the image in (a). A single Gaussian events peak is not visible because there are too many split pixel events, which creates a tail in the histogram to the right of the dark peak.

3.0 The CCID 22.5 Sensor

The digital imaging device used in this experiment was fabricated at Lincoln Labs [3]. It consists of an array of 512 × 516 pixels. The pixels have the dimensions 15 µm × 15 µm. It is a three-phase, back-illuminated, buried n-channel device on a high resistivity p-type silicon bulk substrate.

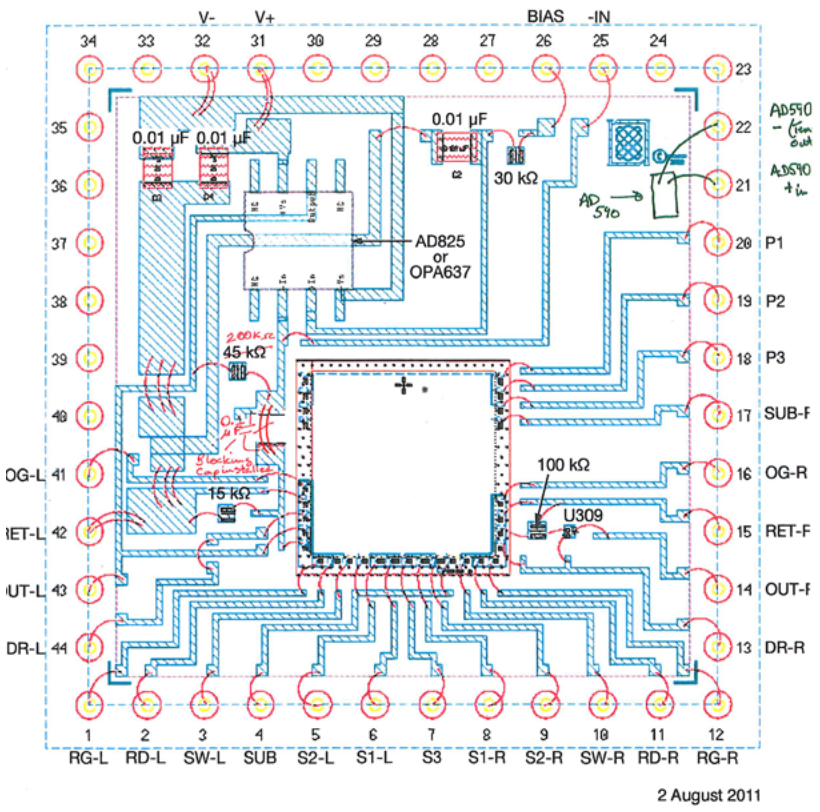


Figure 3.1: Bonding diagram of the CCID-22.5 [3].

A buried channel device is one in which accumulated charge packets are stored and transferred within a channel underneath the Si/SiO_2 interface. Buried channel devices reduce the effect of charge trapping seen in surface channel devices [16].

The AD590 temperature sensor has been fitted to pins 21 and 22 of the CCID 22.5 (Fig. 3.1). All the temperatures in this study were measured using the AD590, which has a resolution of $\pm 0.5°C$ [5].

As shown in Fig. 3.2, it is capable of bi-directional read out, which is set by the clocking of the serial gates S1 and S2.

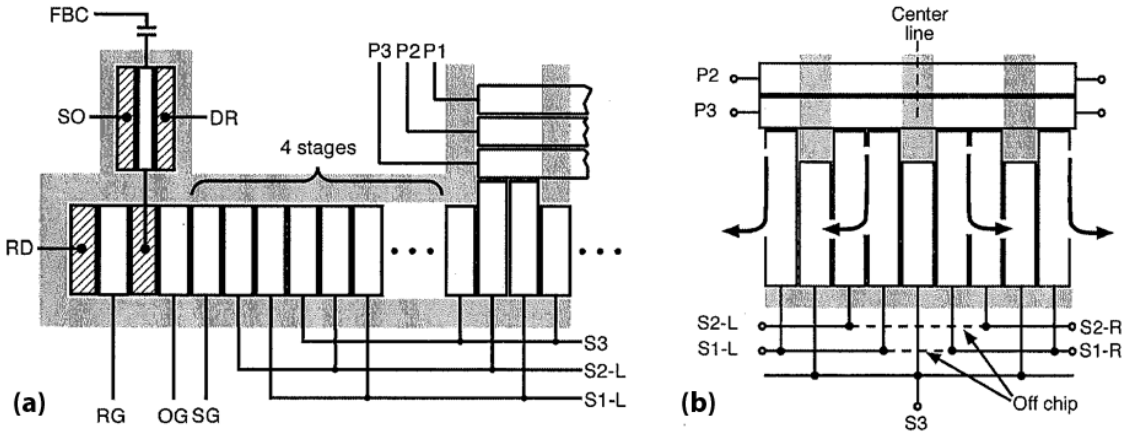


Figure 3.2: The output structure of the CCID-22.5 [3]. (a) The left output of the CCD, which leads to the CFA. (b) The parallel/serial gate interface.

The CCID 22.5 has been fitted with two output structures. The first is a traditional MOSFET source follower configuration similar to Fig. 1.7, with a 100 kΩ load resistor. The other side of the chip has a CFA as illustrated in Fig. 3.3. Having both kinds of outputs on the same chip allows simultaneous testing under the exact same environmental conditions. The two amplifiers differ in the output MOSFET gate dimensions. The source follower output MOSFET has a gate width to length ratio of W/L=25 µm/2 µm and the feedback amplifier side has a ratio of W/L=10 µm/2 µm. The values of the resistors in Fig. 3.3 are R_L=15 kΩ, R_b=30 kΩ, and R_f=45 kΩ. The

amplifier used the AD825 opamp.

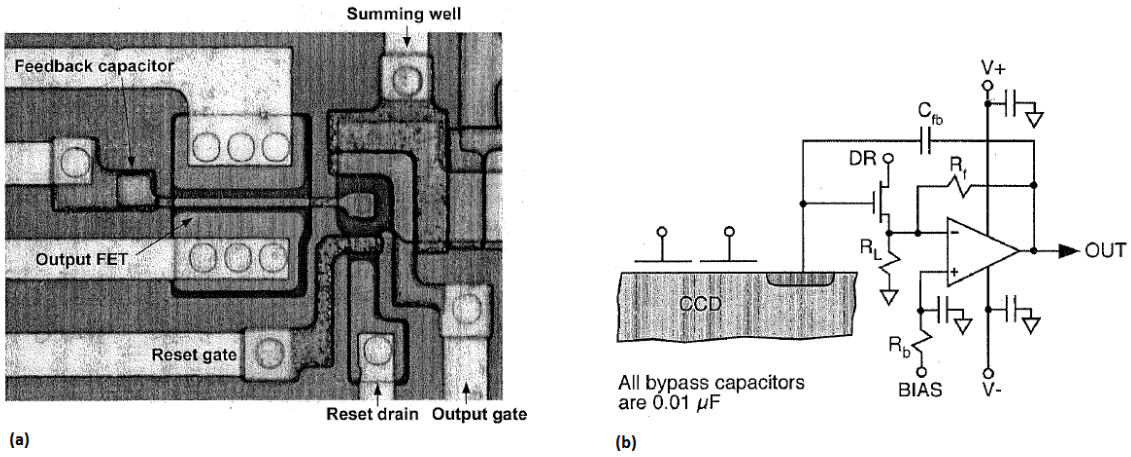


Figure 3.3: (a)Photo of the output of the CFA side of the CCID 22.5 that shows the feedback capacitor. (b) The output circuit diagram of the CFA. The output MOSFET and the feedback capacitor are located on the chip. All other components are off the chip. Note that the reset transistor is on the CCD and not pictured in (b).[3]

Comparing Figs. 1.8 and 3.3 it can be seen that the amplifier in the CCID 22.5 is composed of an output MOSFET and an opamp. In the *Introduction* section, two assumptions were made about an ideal CFA.

1. The input of the amplifier draws zero current.

2. The open loop gain of the amplifier is infinite.

Both of these assumptions hold for the amplifier in the CCID 22.5 CFA. Firstly the MOSFET gate draws no current. While the AD825 is not an ideal opamp and therefore does not have an infinite open loop gain, it does have a very large gain. So the approximation $A \to \infty$ used in Eq. 1.13 is still valid.

3.1 Preliminary Results

The preliminary results from Lincoln Labs showed that the CFA was capable of handling a large range of charge packets (Fig. 3.4). The dynamic range of the CFA is approximately one million electrons, while the SF range is less than 200,000 e^-. The full well of the CCID 22.5 pixels is much smaller than the dynamic range of the CFA, which could only be saturated by binning multiple pixels. Based on the slope of the linear region of the CFA output, the sensitivity was estimated to be S_V=20.8 µV/e^-. Using Eq. 1.13, the feedback capacitor was estimated to be C_{fb}=7.7 fF.

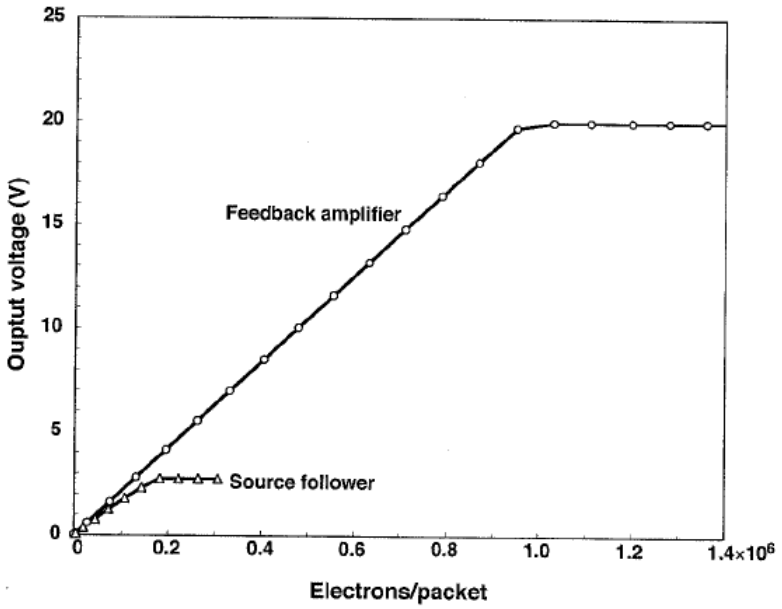


Figure 3.4: Linear transfer of the SF and CFA sides of the CCID 22.5 as measured by Lincoln Labs [3].

The linearity of the CFA was measured by finding the percent deviation from the least square fit of the data in Fig. 3.4. The initial results showed that the CFA had a deviation from linearity of ±4% over its dynamic range (Fig. 3.5). The was partially attributed to the instrumentation available at the time for measurements.

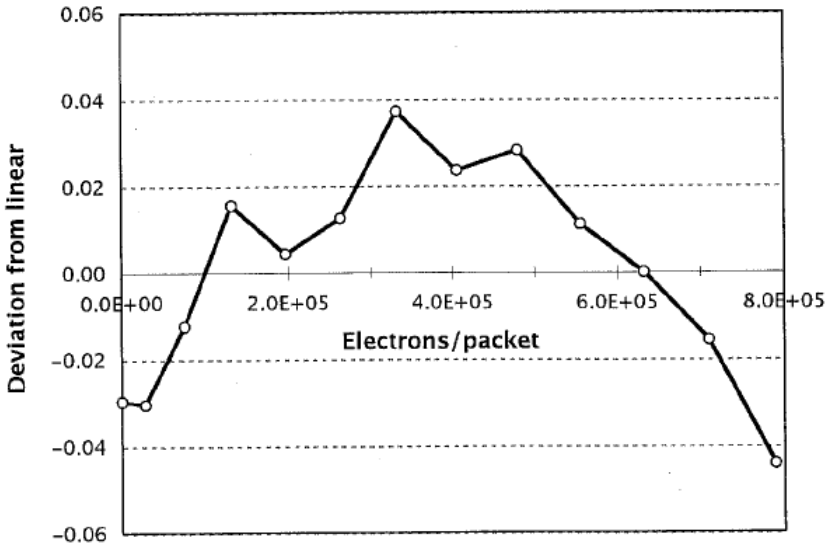


Figure 3.5: Least square fit data of the linear transfer of the CFA side of the CCID 22.5 as measured by Lincoln Labs [3].

4.0 CCD Test Station

The experiments on the CFA and SF outputs required the development of a camera system. A camera was assembled, which comprised of both original and modified equipment and software. The CCD was driven by a Field-Programmable Gate Array (FPGA) and voltage level shifter adapted from a PixelVision camera controller (Fig. 4.1). A DC power supply was used to control the rails of the operational amplifier in the CFA (Fig. 3.3) and a pulse train generator powered the light source, a box containing an array of LEDs. The CCD was kept in a vacuum chamber and cooled using a cyrostat and a cold finger. Lincoln Labs manufactured a circuit board to buffer the CCD signal before being read by the DAQ. Data was collected using a National Instruments PCIe-6361 DAQ. Data acquisition and analysis was done through original LabVIEW code collected in the TDC Suite. Each of these components will be discussed in this section.

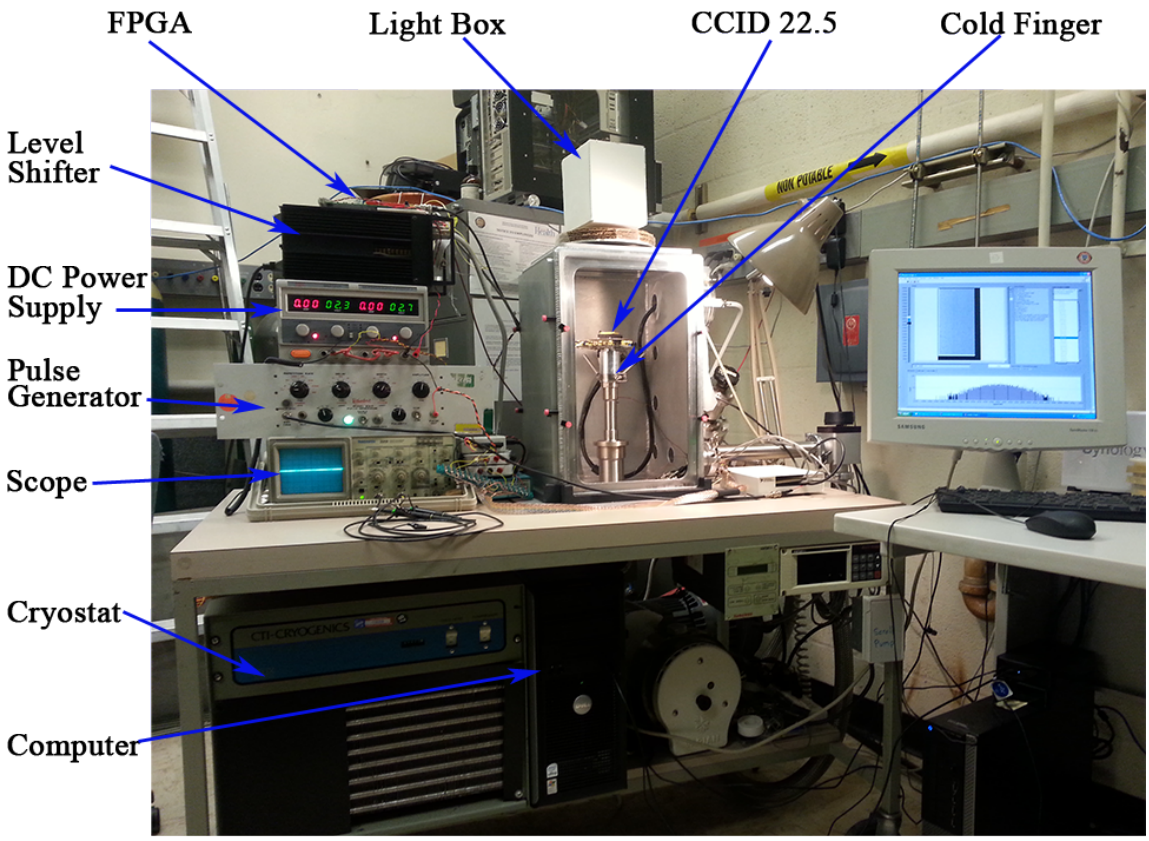


Figure 4.1: CCD Test Station

4.1 FPGA

All AC voltages that control the CCID 22.5 are generated with the Altera Cyclone FPGA [2], which is controlled using Quartus II software. The code that controls the FPGA was developed by John Fastabend and has been detailed in his Master's project report [6]. Only the important details of the Quartus code are described here as well as those which have been modified.

There are ten different states the FPGA uses to *control* the CCD. A state corresponds to a different function of the CCD (Table 4.1). Stare is used while the CCD is being exposed to a light source, charge_dmp1 is used to shift out the dark signal in

the serial register, etc. Each state lasts a specified number of cycles as measured by the FPGA's clock. For a single clock cycle, each output signal of the FPGA may only be either high or low. While in a single state, the FPGA output pattern is repeated and can only change by switching to a new state. The FPGA outputs TTL signals with an amplitude of 3.5 V. The level shifter in Fig. 4.1 increases the amplitude of the driving signals. The amplitudes can be modified by adjusting potentiometers connected to each signal.

CCD State	Function
stare	integrate signal
charge_dmp1	shift dark signal out of serial register
move_line1	shift charge down into serial register
move_line2	shift charge down into serial register
move_line3	shift charge down into serial register
move_line4	shift charge down into serial register
move_line5	shift charge down into serial register
move_line6	shift charge down into serial register
output_row_bin	shift charge into summing well
output_row	shift charge into sense node

Table 4.1: States of the FPGA

After the charge is collected in the CCD, it is shifted into the serial register then moved into the summing well. The summing well can be clocked to collect the charge from one or more pixels. In this way pixels can be combined or binned. The number of pixels that are binned can be modified by changing the value of the variable end_bin in the file 64x64.tdf, which contains the Quartus II code. The data collection software described in a later section offers a Graphical User Interface (GUI) method to change the number of binned pixels as well.

4.2 LED Light Source

The light source consists of an array of high intensity Light Emitting Diodes (LEDs) inside a white enclosure (Fig. 4.2). The light from the LEDs reflects off the white interior of the box and passes through the diffusing screen before exiting. This is done to produce a uniform flat field. The light box contains red (624 nm), blue (470 nm), green (527 nm), and white LEDs, which can be used individually or in combination. Multiple wavelengths of light allow for experiments in CCD quantum yield.

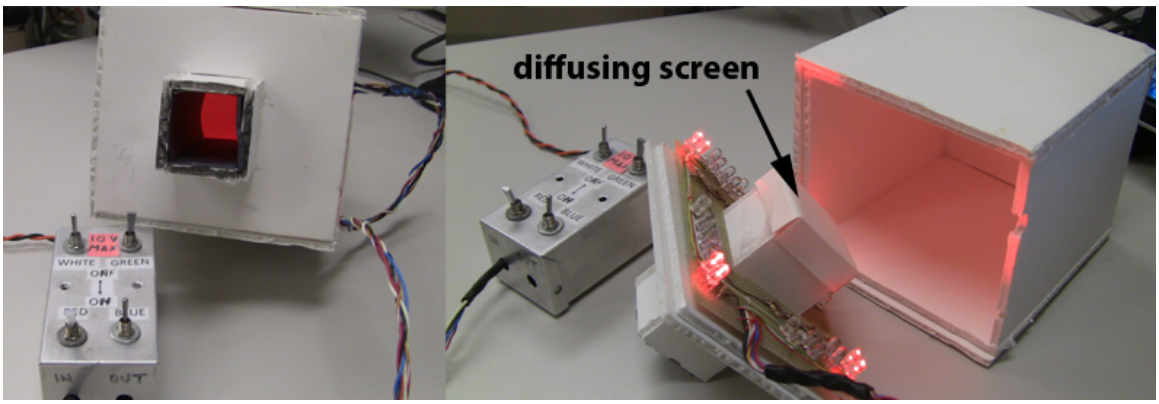


Figure 4.2: Light source

One of the goals of this project is to measure the linearity of the CCD output. This requires being able to produce a consistent pulse of light. The light source is powered by a Rutherford B15 R Pulse Generator, which is triggered by a signal from the National Instruments DAQ. Therefore, the duration and voltage of each pulse is controlled by the pulse generator hardware, and the number of pulses by the LabVIEW software. (See the Data Collection section for more information on LabVIEW.)

4.3 Vacuum Chamber and Cold Finger

This experiment requires that the CCD is cooled to temperatures as low as -110°C. To avoid damage due to condensation, all tests are done inside a vacuum chamber held at a pressure of approximately 10^{-3} torr. Inside the chamber, the CCD rests on a cold finger connected to a cryostat (Fig. 4.3). A sheet of indium foil was used to maintain thermal contact between the CCD and the cold finger.

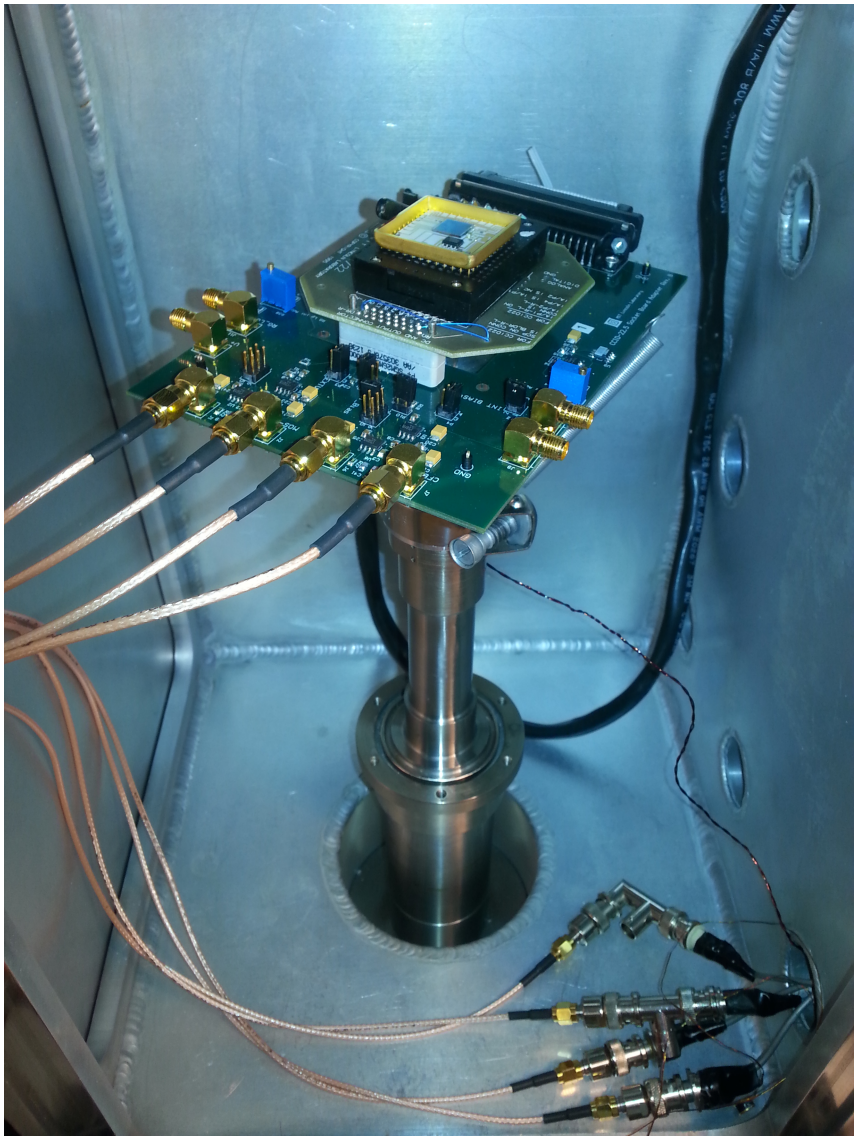


Figure 4.3: The CCID 22.5 chip in on the cold finger the vacuum chamber.

The temperature decreases too rapidly to collect images during the cooling down period, so all data is collected while the cold finger warms back to room temperature. Figure 4.4 shows the temperature of the CCID 22.5 chip as measured by the AD590 (See Fig. 3.1). The number of data points that can be collected for a given temperature is limited by the rate at which the temperature increases. The most rapid increase occurs immediately after the cryostat is turned off and the CCD begins to warm. During this period the CCD warms at a rate of roughly 1.6°C/min.

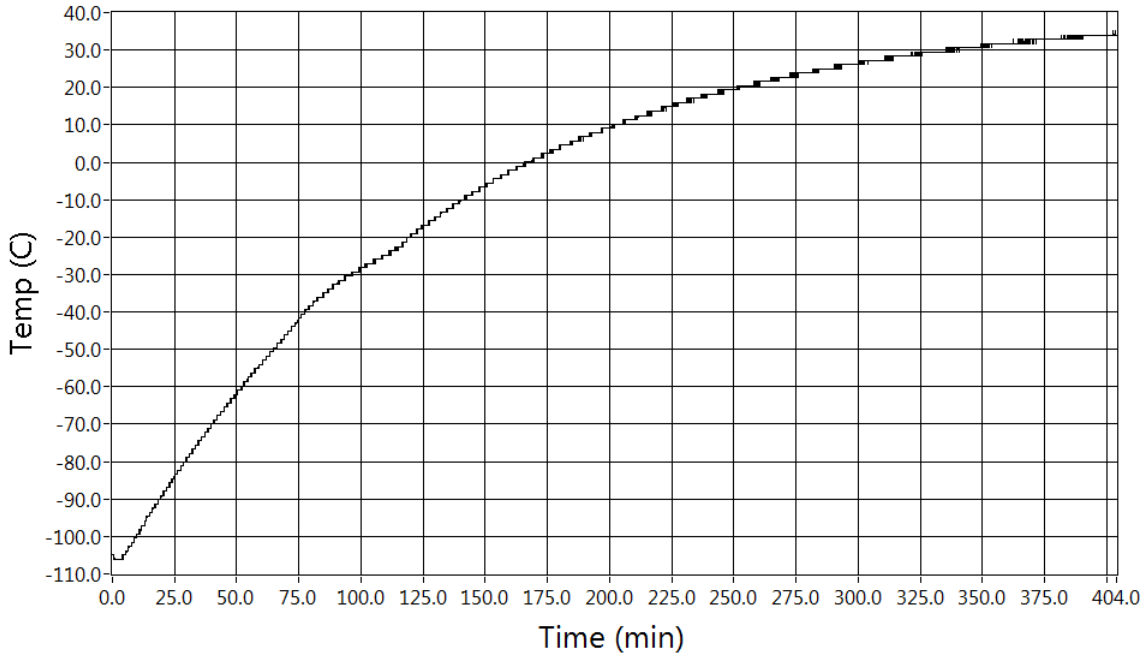


Figure 4.4: Temperature of the CCID 22.5 after it had been cooled to -105°C and allowed to warm. The CCD warms past room temperature due to the heat generated during the operation of the imager.

4.4 Signal Processing

The CCID 22.5 chip is mounted in a signal processing board manufactured by Lincoln Labs (See Fig. 4.3).The purpose of this circuit is to amplify and buffer the signal before being read by the DAQ. The circuit diagrams of the SF and CFA outputs are

shown in Figs. 4.5 and 4.6. A series of jumpers on the board control the direction of the readout of the CCID 22.5: clocking to the SF output, the CFA output, or both. The jumpers labeled P10, P1, and P2 can be used to modify the gain of the signal processing chain, which will be usefull in future studies for studying small signal variations. The board also contains circuits to control the reset function of both amplifiers and the signal processing of the AD590 temperature sensor.

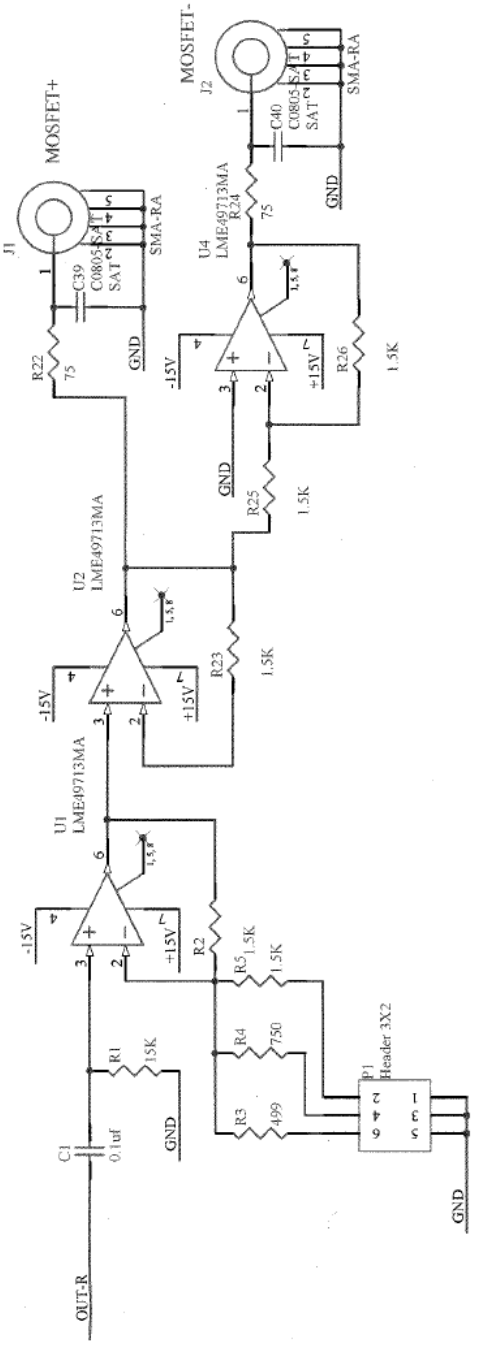


Figure 4.5: Signal chain of the SF output

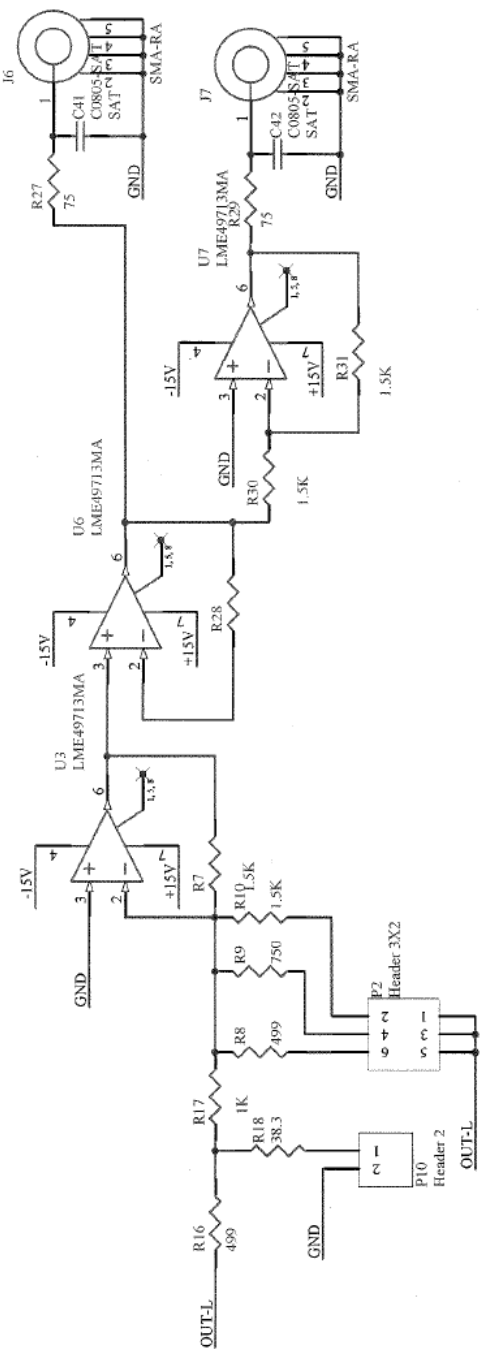


Figure 4.6: Signal chain of the CFA output

4.5 LabVIEW Software

Other than the FPGA, which is programmed with Quartus II software, and the dual DC power source that sets the rails of the opamp in the CFA, all aspects of the camera are controlled using LabVIEW. The TDC Suite contains all the LabVIEW code written to collect and analyze data. LabVIEW is a graphical programming software, which means that code can not be easily represented in text format. In the description of the code written to collect and analyze data, this thesis will rely primarily on simplified block diagrams of the sub routines and screen shots of the GUI and original code. It is assumed that the reader has basic experience with LabVIEW.

Data Acquisition Software

The top level program for data acquisition is Data Collect Main.vi (Fig. 4.7). (.vi is the extension for LabVIEW files and stands for virtual instrument.)

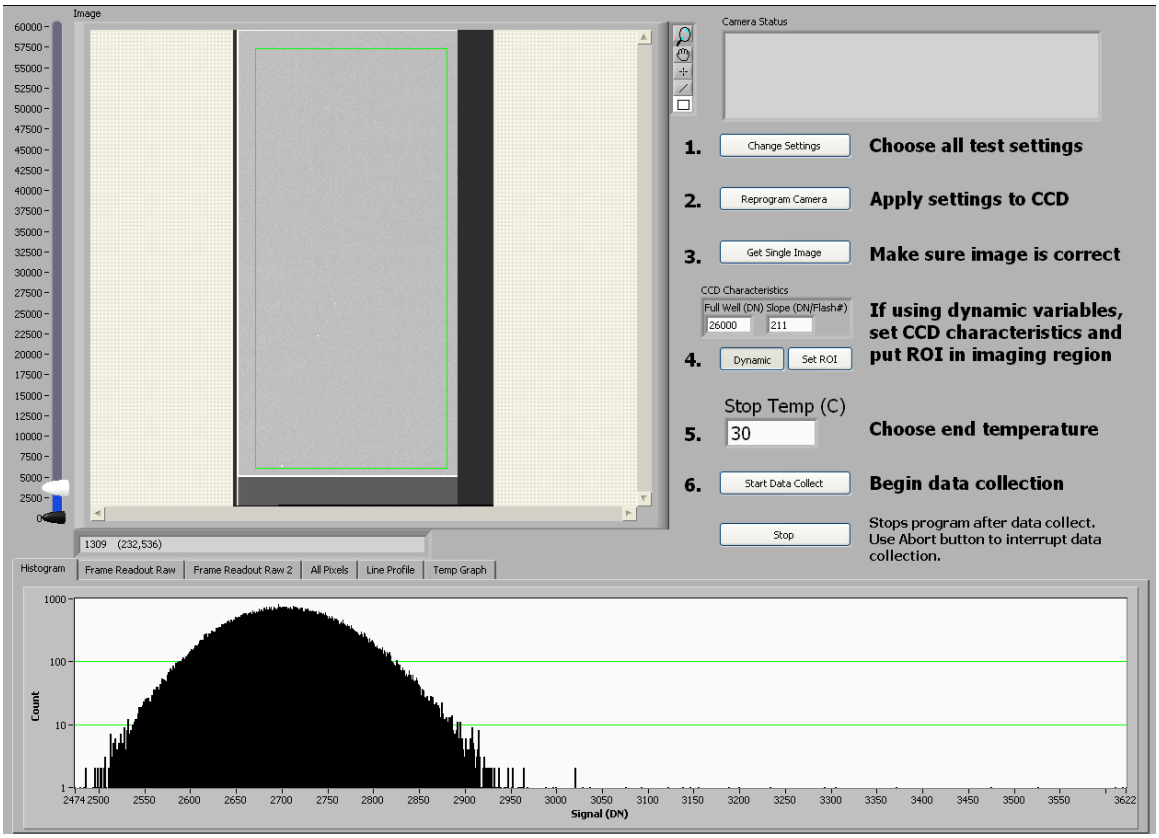


Figure 4.7: Front panel of Data Collect Main.vi

The first step in data collection is configuring the test settings (Fig. 4.8), which can be done from the front panel of Data Collect Main.vi. Change Settings.vi controls all variables associated with the FPGA, the DAQ, and the pulse train generator used to drive the LED light box. Note that the LED color, voltage, and pulse duration options are only for keeping records on the experiment. All of these settings must be changed on the pulse generator or light box directly and cannot be changed by LabVIEW.

All of the values in the Camera Settings cluster box are constants throughout the experiment except for the experiment variable, which is chosen based on the Choose Test Type Selection. The TDC Suite can perform experiments in which the

LED flash count or the CCD integration time is the variable. The Variable Settings cluster box controls the range and increment of the selected variable. For example, the test settings in Fig. 4.8 indicate that the experiment variable is the number of LED flashes. Each flash has a constant pulse duration of one millisecond. The first collected image will correspond to zero LED flashes. The LEDs will flash four times for the next image, eight times for the third image, and so on up to 100 flashes for the 25^{th} image.

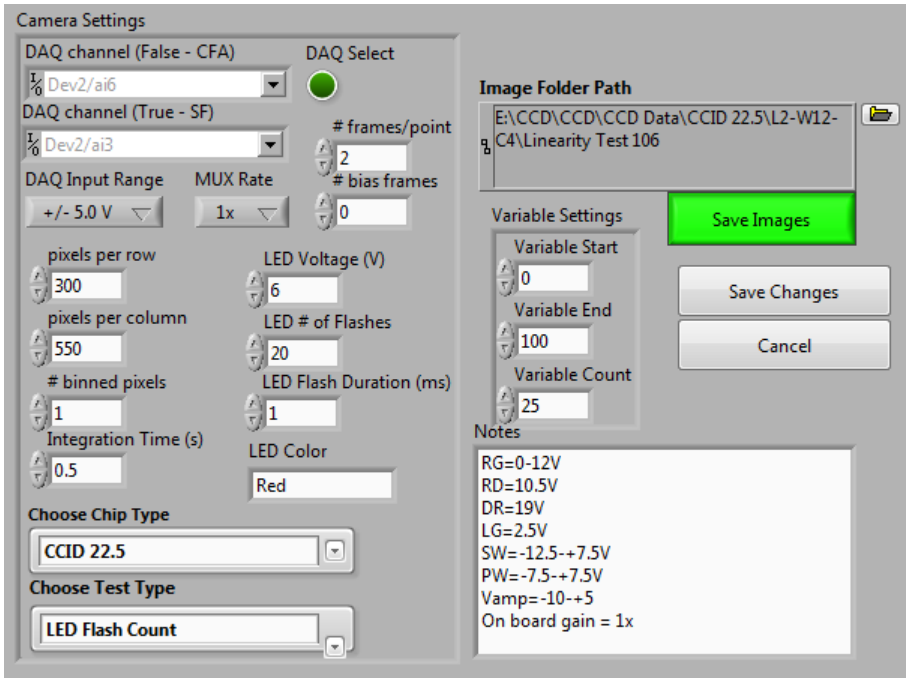


Figure 4.8: Front panel of Change Settings.vi

The main data collection VI is composed of three loops (Fig. 4.9). Loop 1 loads global variables that are modified during the experiment and saved in a separate VI. Loop 2 responds when the user interacts with the front panel of the VI. Examples include collecting a single sample image, changing test settings, and reprogramming the FPGA. Both of these loops are fairly basic and should be readily understood by someone with experience in LabVIEW. Loop 3 controls the actual data collection and

will be the only loop discussed in detail here.

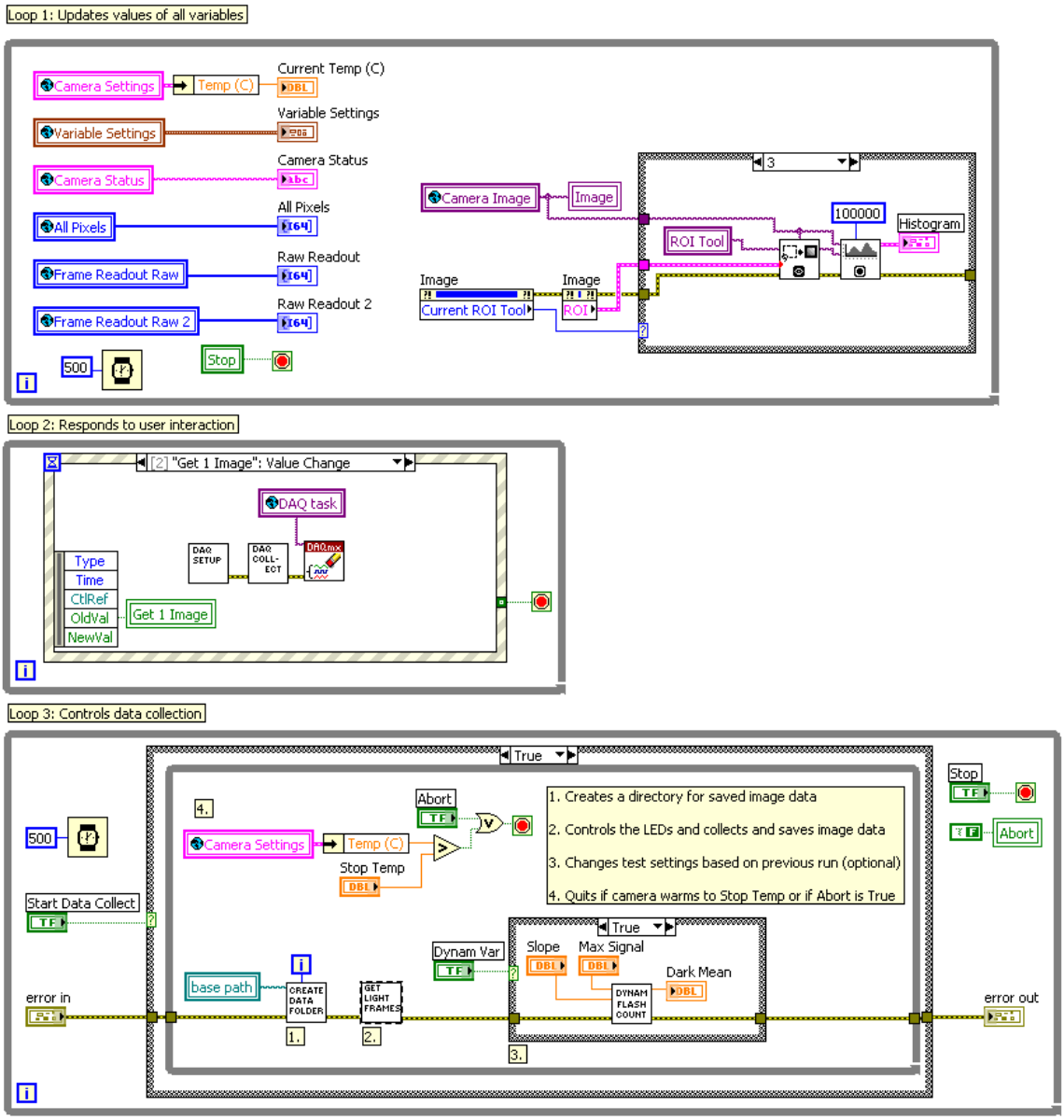


Figure 4.9: Block diagram of Data Collect Main.vi.

The data collection loop begins by creating a directory to save the image data in a file with a comma separated values (CSV) format. The next sub program, Get Light Frames.vi, flashes the LEDs and collects and saves the image data. The final step changes the LED flash count settings after each run (see explanation below).

These steps are repeated until the CCD temperature is greater than the constant Stop Temp, which is set by the user before the experiment.

Get Light Frames.vi

Get Light Frames.vi collects all the data for a single run. In Step 1 (Fig. 4.10) the LED or FPGA setting that is the experiment variable is changed based on the test settings and the iteration of Loop A. For this experiment, the only setting used as a variable is the LED flash count.

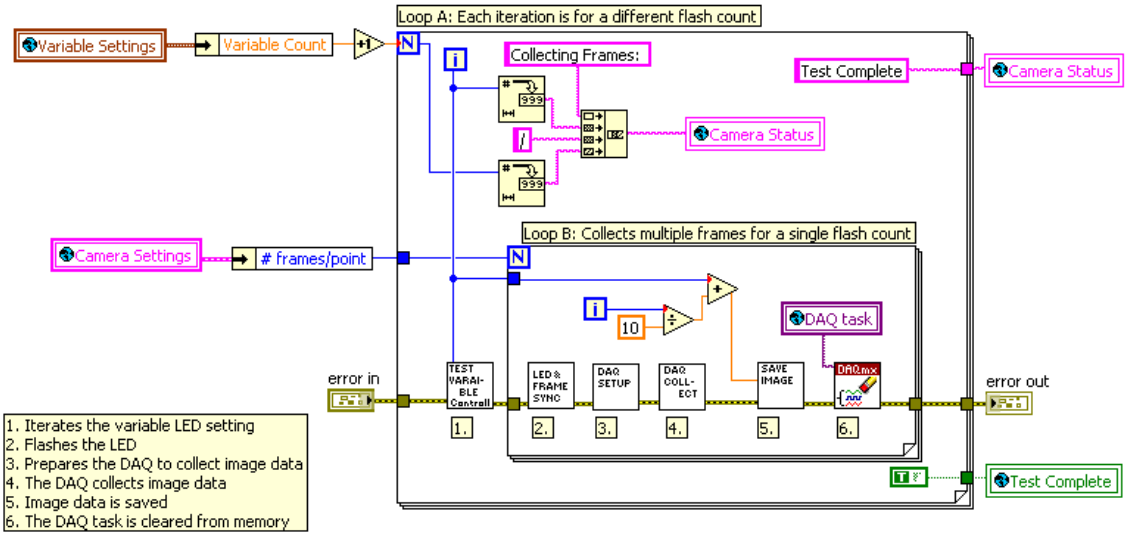


Figure 4.10: Block diagram of Get Light Frames.vi.

Step 2 calls LED and Frame Sync.vi, which ensures that the LEDs flash at the beginning of the *stare* state and not during charge read out (Fig 4.11). This is accomplished using two output pulses from the FPGA: Trigger and Line Sync. During the *stare* state, in which the CCD accumulates the signal from the LED, the Trigger pulse is high and the Line Sync pulse is low. During all other CCD states, Trigger is low and Line Sync is high. LED and Frame Sync.vi first waits until the Line Sync is

high, then waits for the Trigger pulse to go high, indicating that the *stare* state has begun. Without the Line Sync pulse, the LEDs may start flashing during the middle of the *stare* state and continue flashing after the CCD has started shifting the charge. Only once the *stare* state has begun will LED Sub Control.vi be called (Fig. 4.12), which is the VI that sends the trigger pulse to the Rutherford Pulse Generator.

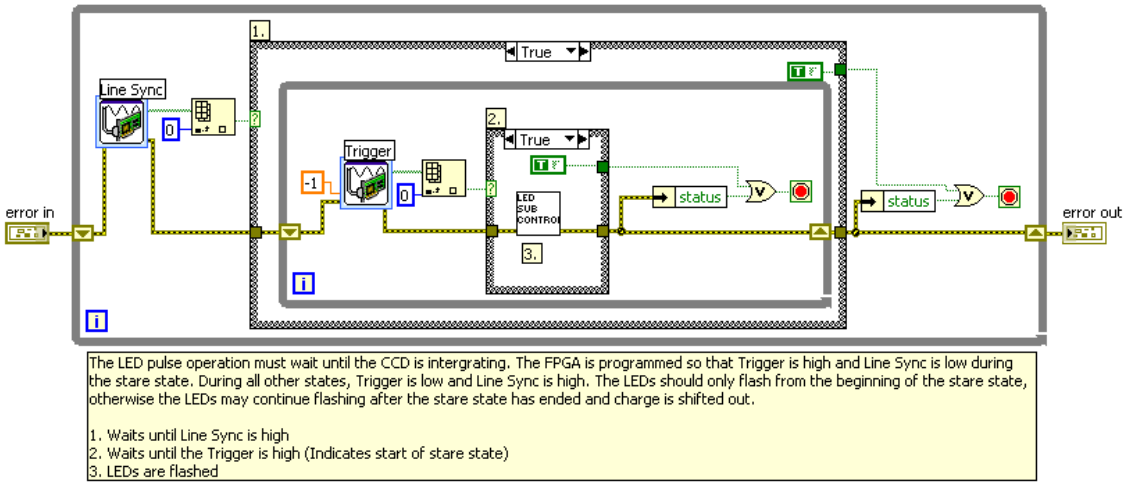


Figure 4.11: Block diagram of LED and Frame Sync.vi.

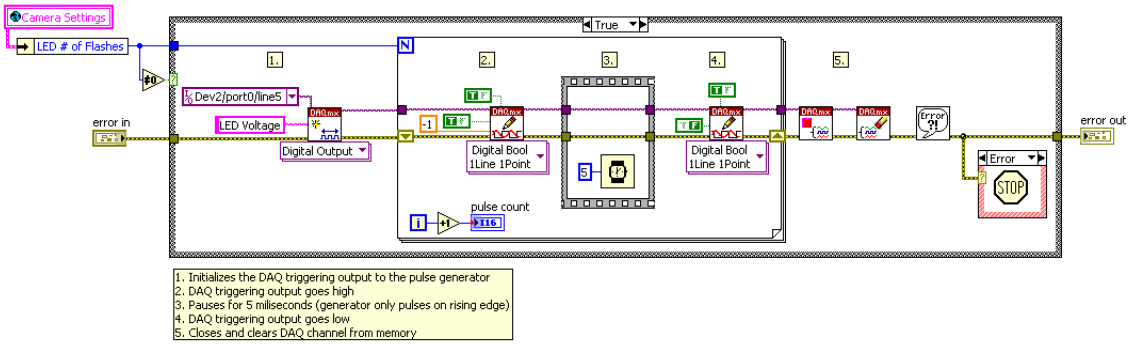


Figure 4.12: Block diagram of LED Sub Control.vi.

Step 3 of Get Light Frames.vi (Fig. 4.10) uses the saved test settings to configure DAQ collection. Step 4 initializes data collection and steps 5 and 6 save the image data and close the DAQ channels respectively.

Dynamic Flash Count.vi

This experiment requires that data be collected across a wide range of temperatures (-110°C $< T <$ 20°C), therefore the level of thermal dark current present in the CCD changes significantly. Because the charge generated by the light source adds to the thermal signal, the dynamic range of the CCD decreases as the temperature increases. The flash count of the LEDs must be modified as the temperature changes to account for this so as to avoid collecting an unnecessary amount of data or, conversely, not collecting enough data to measure CCD linearity. The maximum signal of the CCD is given by

$$Saturation = f_{max} \cdot m + DarkSignal, \tag{4.1}$$

where m is the slope of the CCD Signal vs. LED Flash Count plot (See Fig. 4.13), f_{max} is the maximum number of LED flashes for a test, and $Saturation$ is the full well of the CCD. The program Dynam Flash Count.vi in step 3 (Fig. 4.9) finds the previous dark signal and changes the maximum flash count of the LEDs according to Eq. 4.1. In this way the full dynamic range of the CCD is measured in each run. Note that the slope and full well of the CCD must be measured in advanced. This can be done a single time at room temperature and saved.

Data Analysis Software

Linearity Analysis

There are a number of calculations that can be used in testing the linearity of a CCD, all of which are contained in the program Linearity Analysis Main.vi (Fig. 4.13). The most important calculation for this study is the linear residuals, which is explained

in section 2.1. In addition, this program provides information on the overscan section of the image and the variance PTC.

Before beginning the program, the analysis mode must be chosen. This determines whether the program automatically plots the data fit equations and exports the data to a CSV file. The Auto Analysis button determines whether all the runs within the test are calculated, meaning all the data over the full temperature range, or a single run at a chosen temperature.

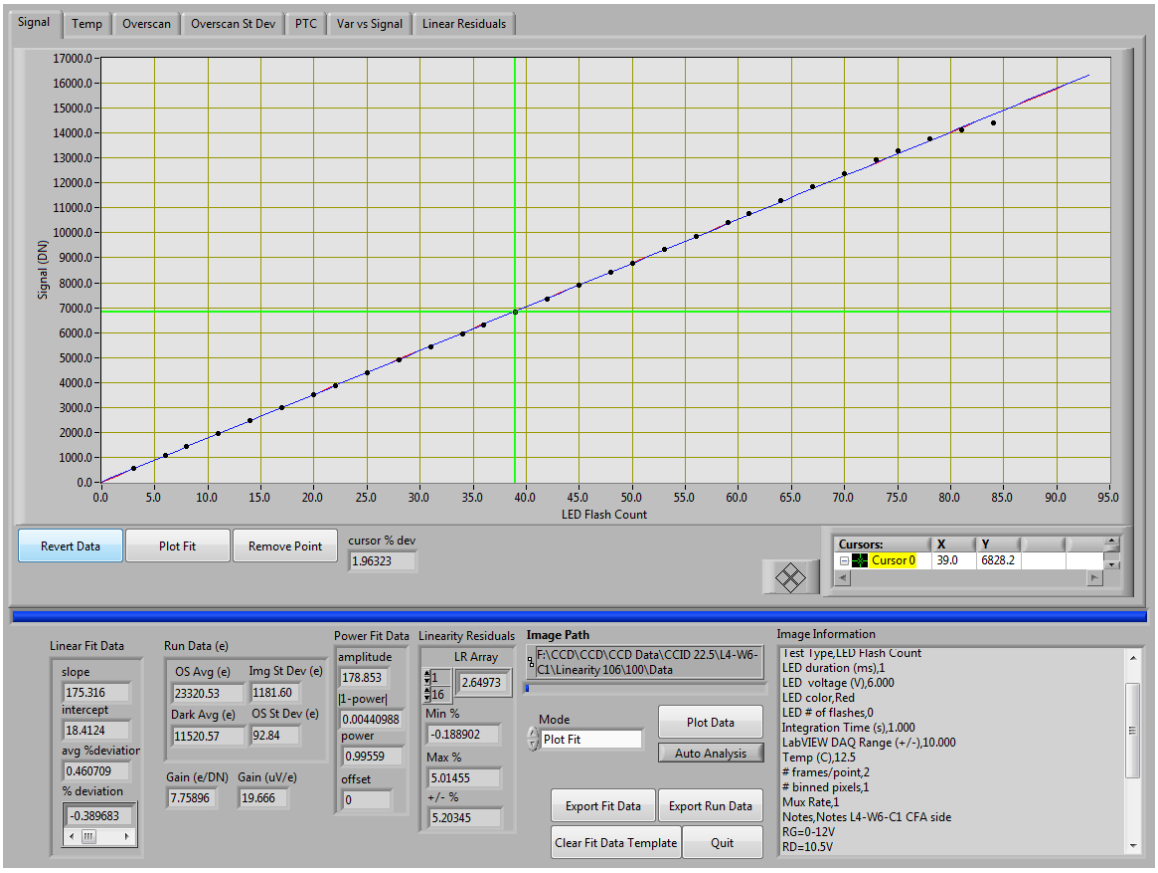


Figure 4.13: Front panel of Linearity Analysis Main.vi.

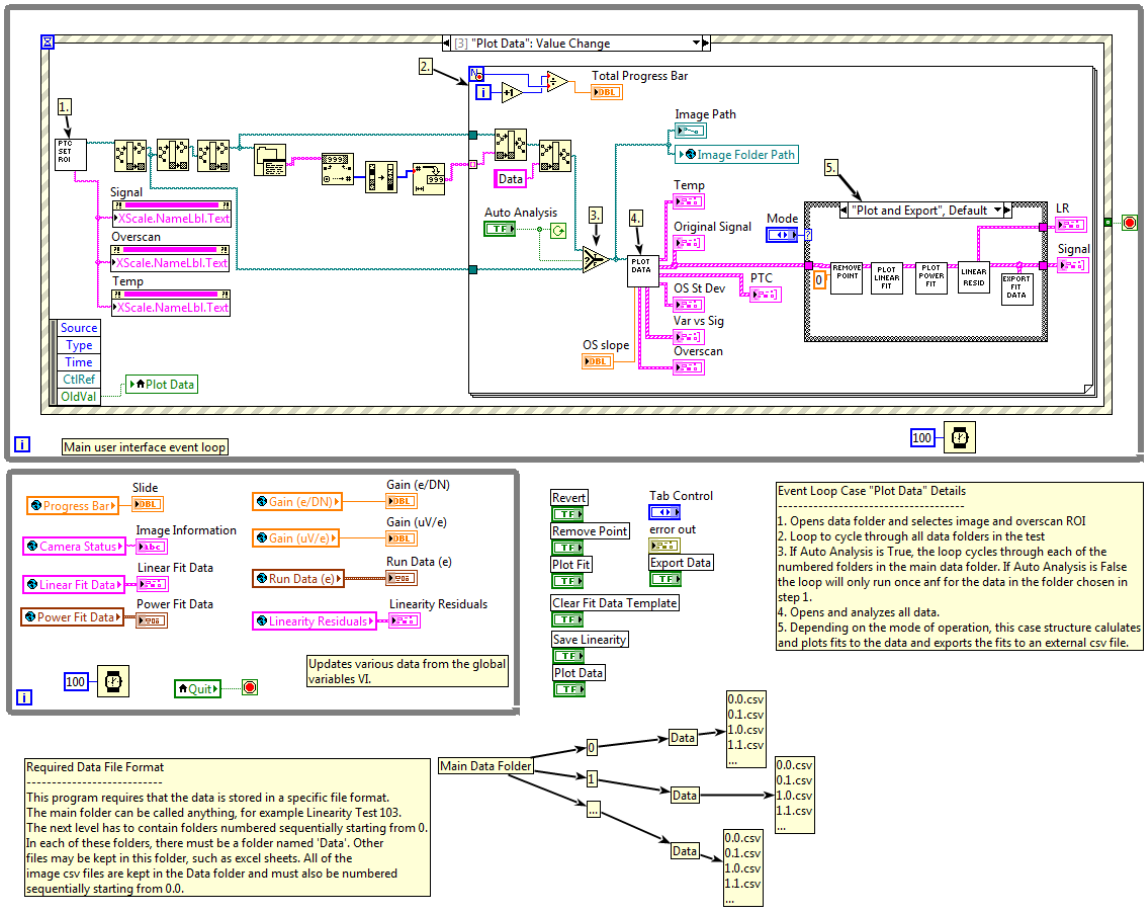


Figure 4.14: Block diagram of Linearity Analysis Main.vi.

Once these options are selected, the program may be started by clicking on the Begin Analysis button. This calls the main loop shown in Fig. 4.14. Step 1 is the program PTC Set ROI.vi (Fig. 4.15), which is used to select the regions of interest of the image for analysis. Both a region in the image area and a region in the overscan must be selected for the analysis. This program also selects which data files to analyze. Once the data and ROI are chosen, the loop in step 2 begins. Each iteration of this loop performs calculations on a single run. If Auto Analysis from the front panel was set to True, this loop would cycle through all the data in the test folder.

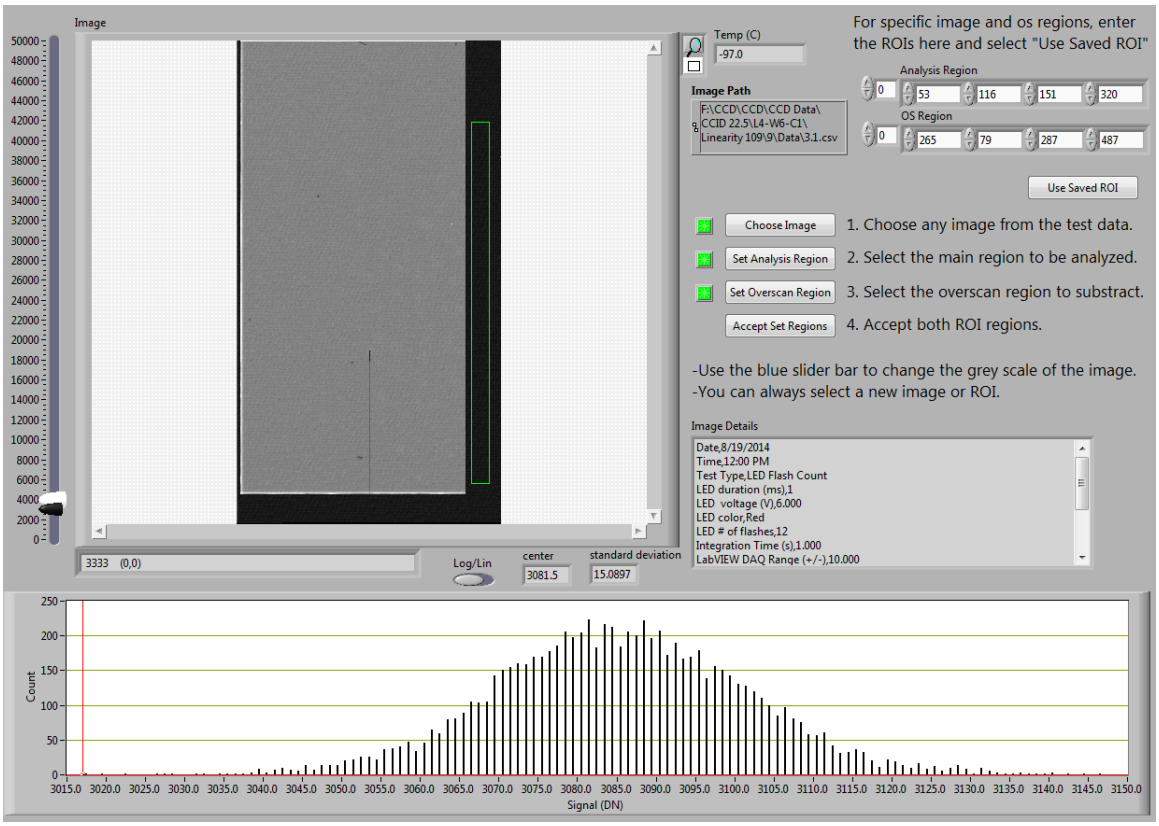


Figure 4.15: Front panel of PTC Set ROI.vi.

Step 3 is the program Plot Data.vi (Fig. 4.16). This program takes the data from a single run and plots all the graphs seen in Linearity Analysis Main.vi (Fig. 4.13) including the variance PTC, which is used in step 4 to calculate the gain of the CCD. This gain calculation is not as accurate as the gain calculated using a radiation source as described in section 2.2, and is used as a comparison and for rough estimation of values in electrons rather than in DN.

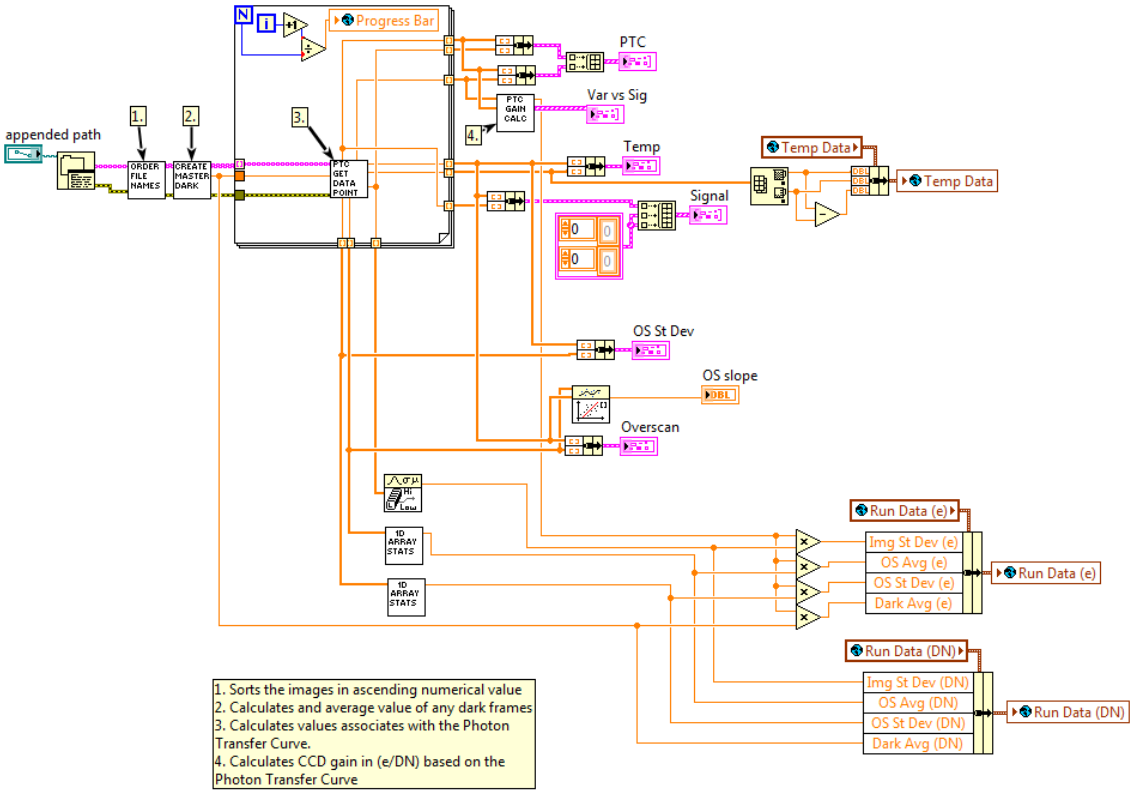


Figure 4.16: Block diagram of Plot Data.vi

Once all graphs are plotted, step 5 calculates the fits of those graphs, computes the linear residuals, and exports the calculated data to a data file depending on the analysis mode chosen on the front panel of Linearity Analysis Main.vi (Fig. 4.13).

Gain Analysis

The purpose of this program is to find the gain of the CCD using the method described in the Experimental Design section (2.2), where the CCD is exposed to a radiation source that produces a known number of e-h pairs. Gain Analysis Main.vi (4.17) handles all steps of the analysis including image addition and Gaussian fitting.

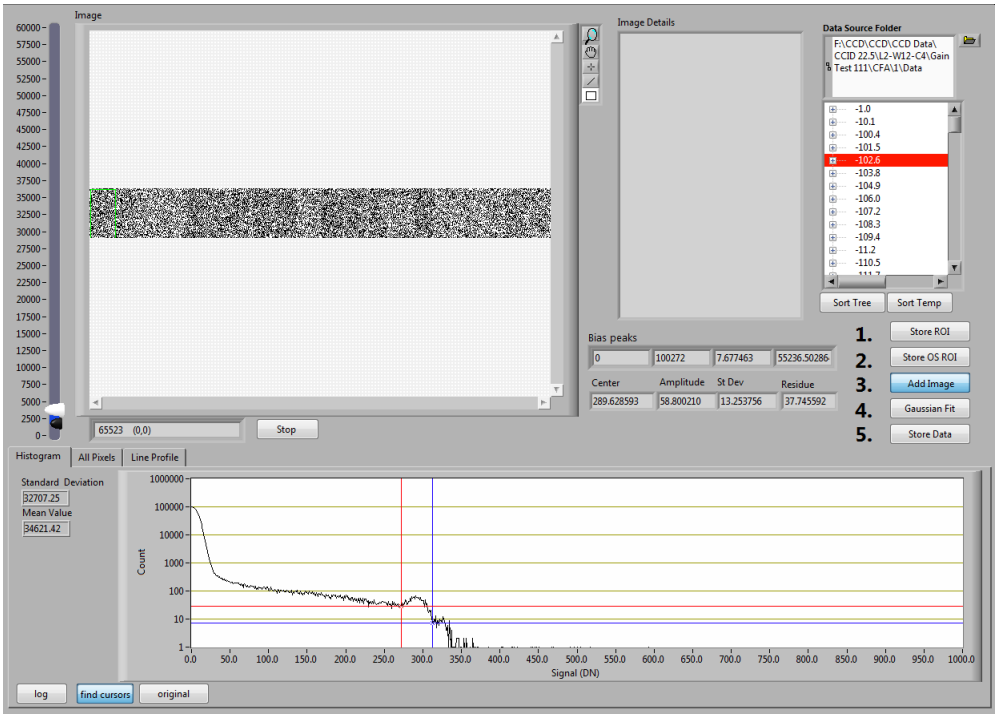


Figure 4.17: Front panel of Gain Analysis Main.vi

The program first arranges all the data files into sub-folders based on the temperature of the CCD when the image was taken. Next the user must select and store the image and overscan ROI (Fig. 4.17). This only needs to be done once. Once the ROIs have been saved, the gain at each temperature can be calculated. This is done by selecting a temperature folder in the tree control and clicking on the Add Images button. The Gaussian fit of the bias peak of each image in the temperature folder is found. The center of that Gaussian fit is subtracted from every pixel in that image, so that the bias peak is now centered at zero. Each of these modified images are combined into one large image, which is returned to the Gain Analysis Main.vi front panel. Finally, the user places the cursors of the histogram around the x-ray events peak, as shown in Fig. 4.17 and clicks on the Gaussian Fit button to find the best fit of the signal. The fit is calculated using standard LabVIEW software and is displayed in a second window (Fig. 4.18). If the fit is acceptable, all data for this temperature

can be exported to an external file by clicking on the Export Data button. The next temperature folder is selected and the process is repeated starting with adding the images in the folder.

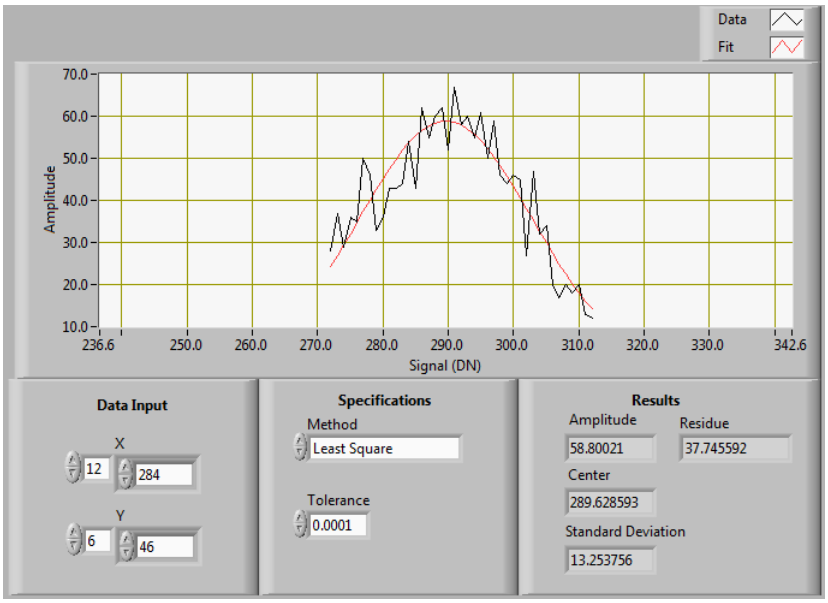


Figure 4.18: Front panel of Gaussian Fit.vi

This procedure is illustrated in Fig. 4.19. Once the fit data for all the folders is found, the data in the external file can be used to find the gain of the CCD versus temperature as described in the section 2.2.

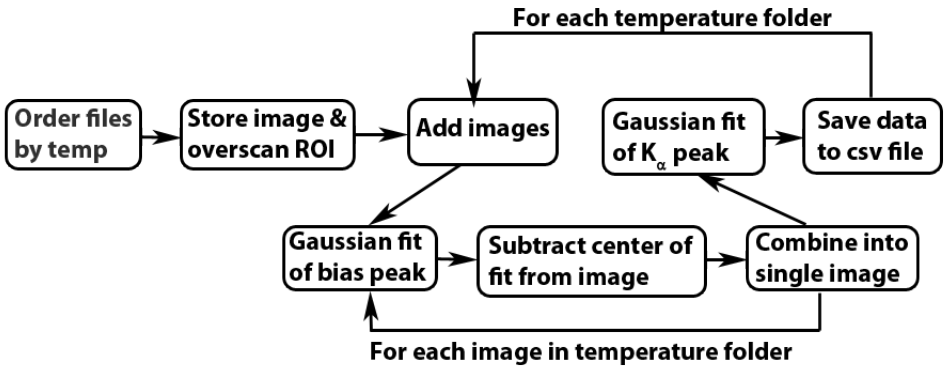


Figure 4.19: Flow chart of the procedure used by the gain analysis software.

5.0 Results

Two CCID 22.5 imagers from Lincoln Labs are used in this study (L2-W12-C4 and L4-W6-C1). Throughout this section they are referred to as C4 and C1. Lincoln Labs found that both chips exhibited threshold shifts in the gates associated with the output structure. The reset gate of C1 is shifted relative to other CCID 22.5 devices, but is able to transfer large signal packets. C1 is still a functional chip used for both gain and linearity testing. However, the threshold shift has compromised the ability of the second chip (C4) to handle large amounts of charge. Because of this, C4 is only used in the gain stability versus temperature tests and not the linearity tests.

5.1 Gain Stability Versus Temperature

The gain for both sides of the imager was measured using an x-ray radiation source as described in the Experiment Design section. The C4 imager was tested with a 5.9 keV FE^{55} source and the C1 was tested with a 23 keV Cd^{109} source. At room temperature the FE^{55} and Cd^{109} sources produce approximately 1620 e^-/photon and 6300 e^-/photon respectively [9]. Cd^{109} has a long absorption length in silicon and many of the x-rays pass through the CCD. In order to record enough events, the charge integration period must be increased. At warmer temperatures ($T > -20°C$), the longer integration time leads to a larger amount of dark current. High levels of dark current limit how well the events peak in Fig. 2.2 can be resolved. Because

of this, the temperature range of the gain tests of the C1 chip were limited to a maximum temperature of -20°C. Cd^{109} was used in the initial gain tests because of its availability, however FE^{55} will be used in future tests.

Gain Measurements

X-ray events in the C1 chip are visible in the images in Fig. (5.1). To maximize the number of x-ray events, the whole imaging area was used to test each output. Because of this, the data for the CFA and the SF amplifiers were not taken simultaneously.

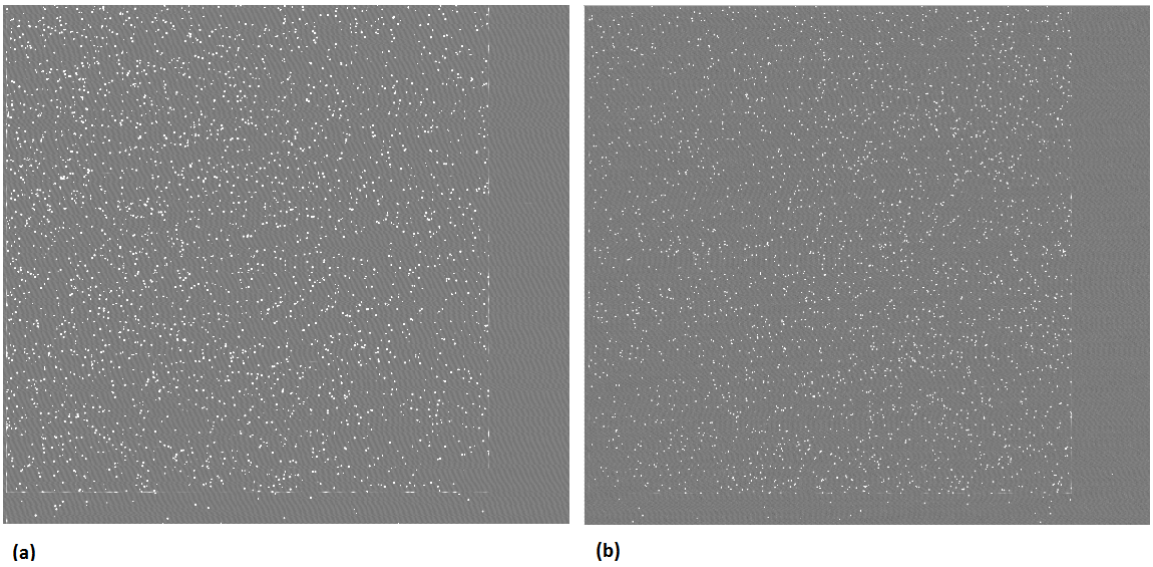


Figure 5.1: Images taken from the (a) SF and (b) CFA sides of the C1 chip while exposed to a Cd^{109} radiation source.

X-ray events in the C4 chip are visible in the images in Fig. (5.2). Instead of using the whole imager for each output, this test read both sides of the chip with the goal of maximizing the number of stackable images aquired at a single temperature. The SF side does not show the same even distribution of events as the CFA. This was caused by improper placement of the source relative to the imager, resulting in fewer

events on the left most edge of the SF side. Despite this, there are enough events to form a discrete events peak as seen in Fig. (5.4(a)).

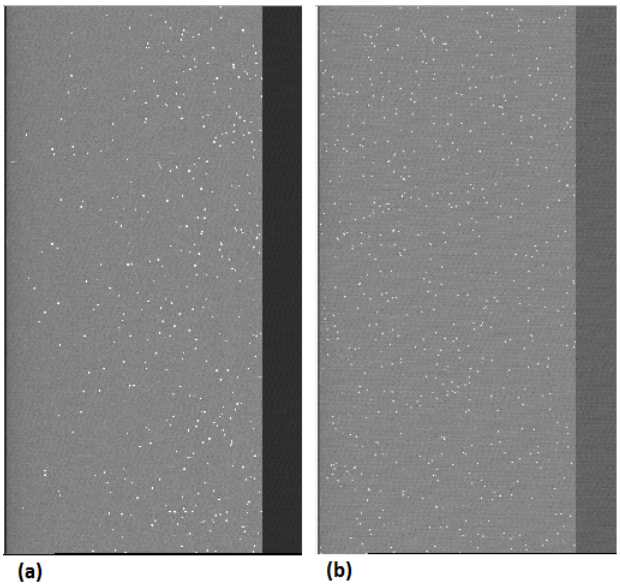


Figure 5.2: Images taken from the (a) SF and (b) CFA sides of the C4 chip while exposed to an FE^{55} radiation source.

All the images taken at the same temperature were added together and a histogram of the combined image was generated. A Gaussian fit was used to find the center of the events peak (Fig. 5.3 and 5.4). The events peak is considerably smaller than expected when compared to published work on calculating gain with FE^{55} or Cd^{109} [9]. This is a persistent issue that could not be resolved by adjusting the camera settings or by using a different type of radiation source. It is unclear why the peaks are smaller, but it may be due to a number of causes including charge diffusion, large read noise, or poor charge transfer efficiency (CTE) [11]. The amplitudes of the peaks were sufficiently large to perform gain calculations.

For both chips the events peak for the SF side has a higher amplitude than the CFA side. This suggests that the CFA output has a larger amount of read noise than the SF output or a poorer CTE.

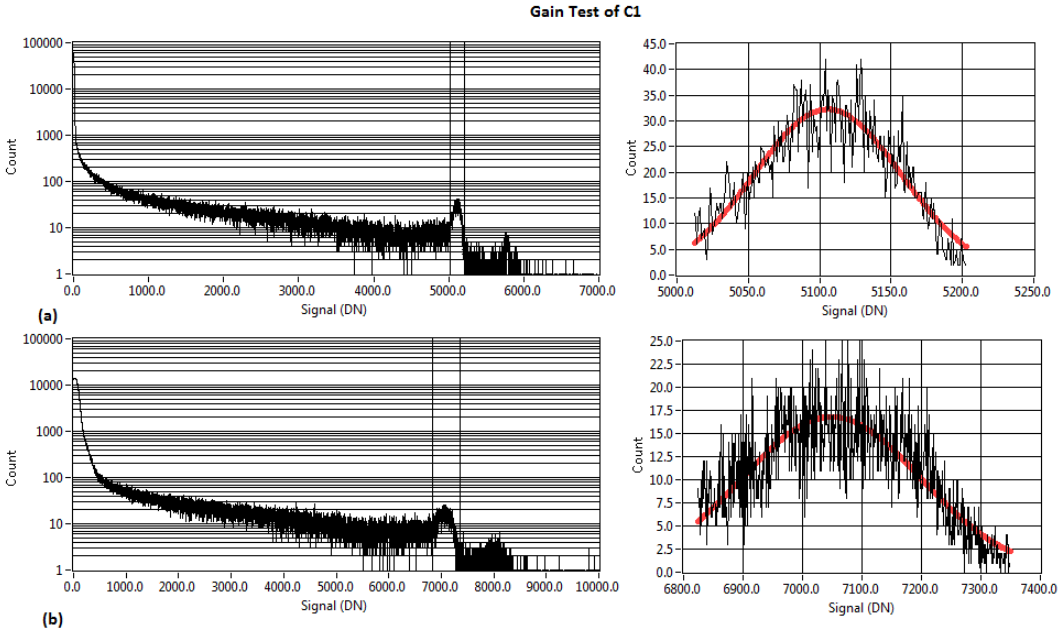


Figure 5.3: Results of the x-ray gain tests of the (a) SF and (b) CFA sides of the C1 imager at -97.0°C. The panels on the left are histograms of the combined images after removing the dark signal. The vertical lines in the histograms mark the position of the events peak and represent the section of data used in the Gaussian fits in the panels on the right.

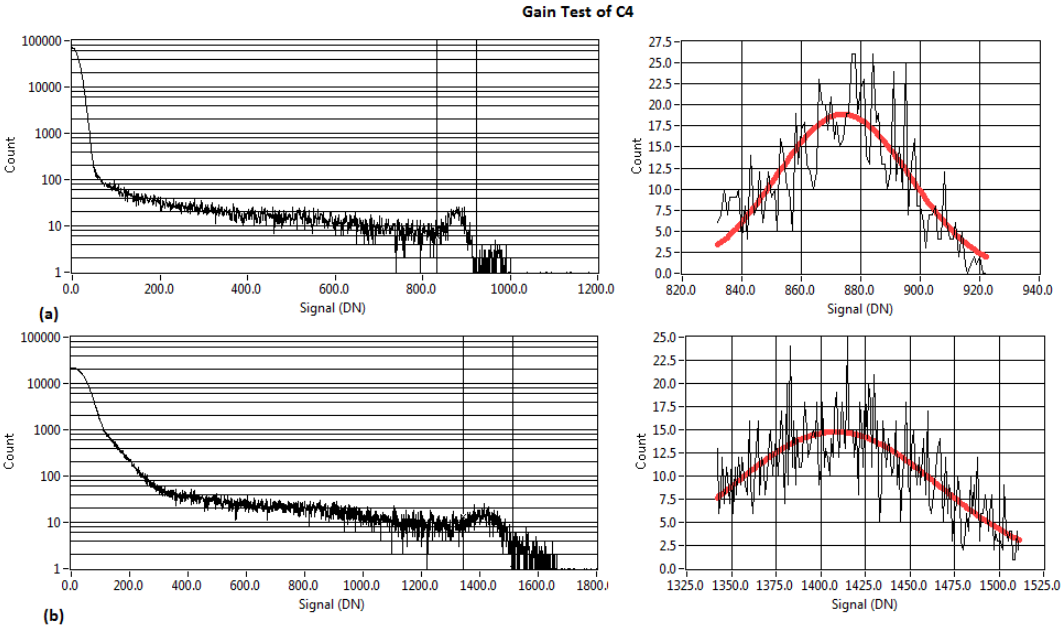
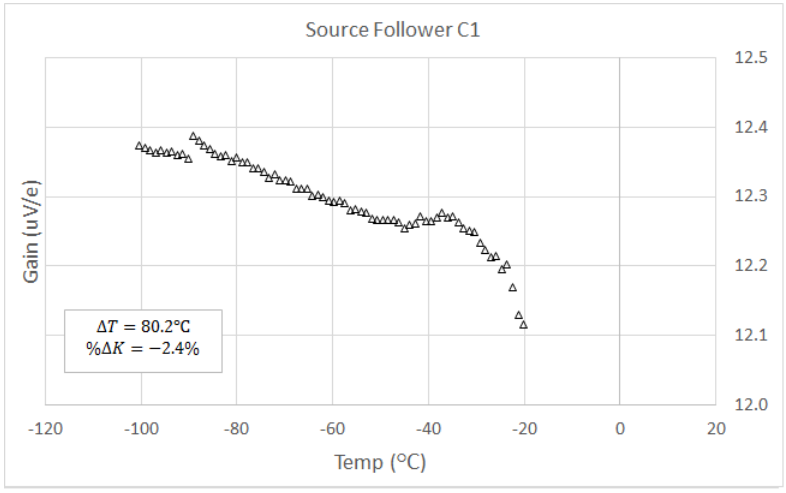
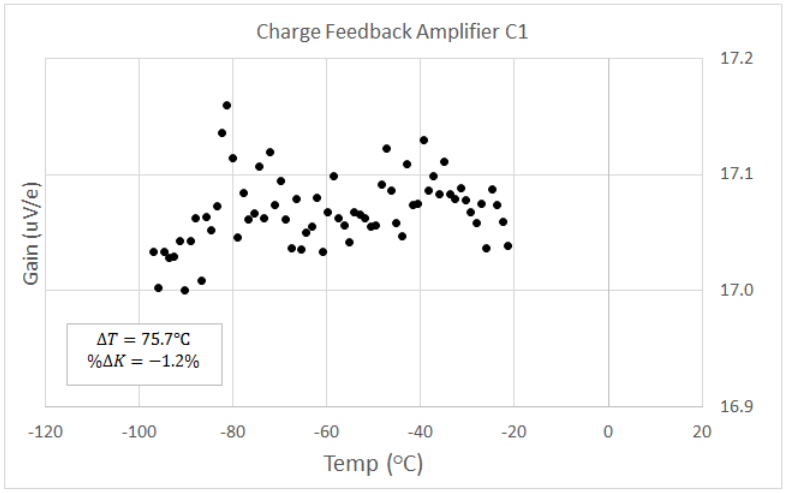


Figure 5.4: Results of the x-ray gain tests of the (a) SF and (b) CFA sides of the C4 imager at -97.0°C.

The x-ray gain calculations of the C1 chip is plotted in Fig. 5.5. It is unclear what caused the discontinuity in the SF gain at -90°C or the leveling out at -45°C. Future testing should reveal whether this is a characteristic of the imager or if it was due to the experimental setup.



(a)



(b)

Figure 5.5: Gain of the (a) SF and (b) CFA outputs of the C1 imager versus temperature.

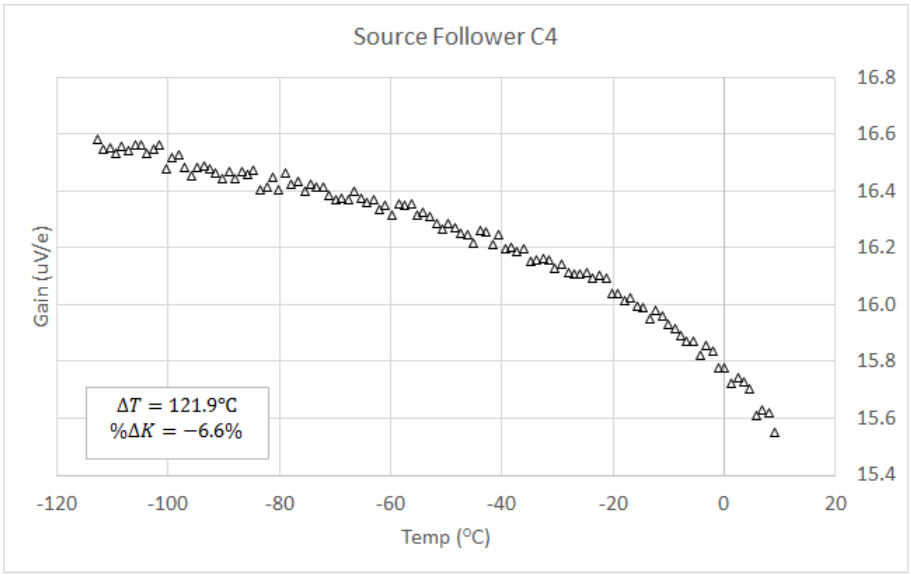
The gain of the SF side of the imager decreases as the temperature increases. The CFA gain seems to increase, though the spread of the data may be obscuring a

downward trend. The change in the SF gain is larger. Changes in gain are quantified using the percent change equation.

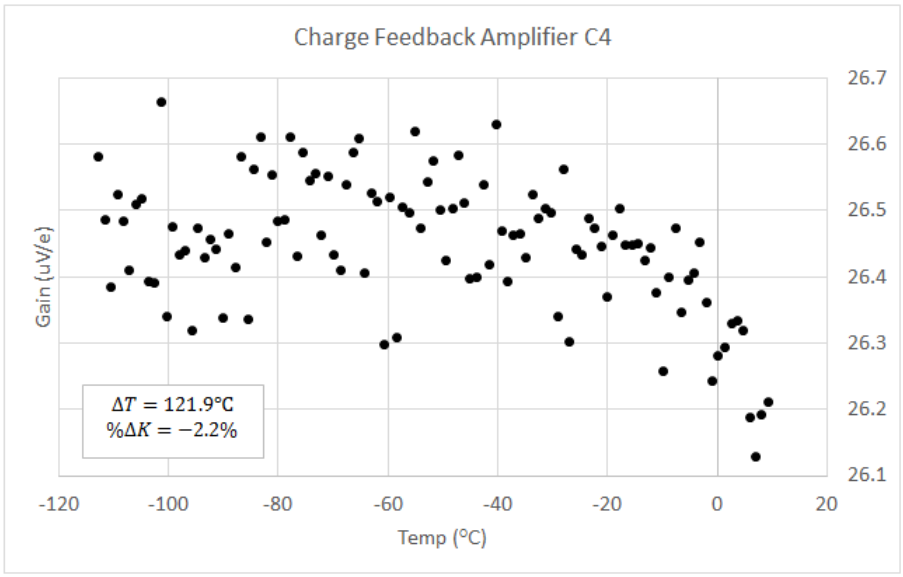
$$\%\Delta K = \frac{K_{min} - K_{max}}{K_{max}} \times 100\%, \tag{5.1}$$

where K_{max} and K_{min} are the maximum and minimum gain values. The SF shows a -2.4% change but the CFA only changes by -1.2%. Because these gains were measured during separate tests, as previously explained, the data does not cover the exact same temperature range. It is possible that the output that was measured over a larger temperature range would exhibit a larger $\%\Delta K$. It will be shown later that if data from the same temperature range is compared, the SF will continue to show a larger $\%\Delta K$ than the CFA.

The x-ray gain calculations of the C4 chip also show a decrease in gain as the temperature increases (Fig. 5.6). Again the $\%\Delta K$ is larger for the SF than the CFA, -6.6% and -2.2% respectively. This data was collected during the same test and over the same temperature range, so the $\%\Delta K$ calculation is not being biased by a greater drop in temperature.



(a)



(b)

Figure 5.6: Gain of the (a) SF and (b) CFA outputs of the C4 imager versus temperature.

Because temperature has an effect on the change in gain for both chips, it is necessary to compare data taken over the same temperature range. Table 5.1 lists the K_{max}, K_{min}, $\%\Delta K$, and the average gain ($\bar{K}$) over the temperature range $-97°$C

$< T < -21.3°C$. This is the largest temperature range common to all tests.

Both chips show a greater percent change in gain in the SF output than in the CFA output. Furthermore, the $\%\Delta K$ of both SF outputs is approximately the same. This is also true for both CFA outputs. The average gains are in close agreement with the preliminary measurements made by Lincoln Labs. Lincoln Labs took x-ray gain data at room temperature, which may play a role in the difference between the their measurements and the data collected in this study.

			$-97.0°C < T < -21.3°C$				
Chip	Source	Output	K_{max} ($\mu V/e^-$)	K_{min} ($\mu V/e^-$)	$\%\Delta K$ (%)	$\bar{K}$ ($\mu V/e^-$)	LL† ($\mu V/e^-$)
C1	Cd^{109}	SF	12.4	12.1	-2.4	12.3	14.0
		CFA	17.2	17.0	-1.2	17.1	18.1
C4	Fe^{55}	SF	16.5	16.1	-2.4	16.3	14.4
		CFA	26.6	26.3	-1.1	26.5	26.5

†All measurements made using Cd^{109} at approximately 30-35°C.

Table 5.1: Comparison of the measured gains of both chips as measured in this study and by Lincoln Labs.

Pair Production Energy

There is a clear trend in the plots on Figs. 5.6 and 5.5 showing that the gain of the imagers decreases with increasing temperature. Equation 1.15 states that the gain of the camera is inversely proportional to the number of electrons generated by an incident photon (η_i). It has been shown that η_i increases with temperature because of it's dependence on the band gap of silicon [4, 14, 13]. Therefore the decreasing gains seen in the imagers could be partially attributed to the change in the band gap of the silicon. Future work will need to focus on determining the relationship between η_i and temperature based on a literature review and further measurements.

Additionally, calculations will need to account for the Fano factor, which is a metric for the uncertainly in pair production due to energy losses caused by non-e-h processes [9].

Read Noise

Referring to the gain vs. temperature graphs, both imagers show a higher spread in the data for the CFA measurements than the SF. This could indicate that while the CFA exhibits a smaller percent change than the SF, the CFA has a higher level of read noise. The read noise of both chips is plotted versus temperature in Fig. 5.7. The read noise was measured in DN and converted using the gains in Figs. 5.5 and 5.6. It is important to remember that due to the temperature dependence of the gain, these values might not be fully accurate. The read noise of the CFA is larger than that of the SF for both chips. Although the C1 measurements do not have a uniform response, there is a clear upward trend in the read noise of both of the CFA outputs as the the temperature increases. The C1 read noise is much larger than in the C4 chip, which could be a characteristic of the imager itself or may indicate that there was another non-uniform noise source, such as electromagnetic interference (EMI), at the time of the test. The C4 SF output shows only a slight increase in read noise at low temperatures. Whether the C1 read noise is also increasing at low temperatures is not discernible because of the large spread of the measurements. This may have also been the result of EMI at the time of the test.

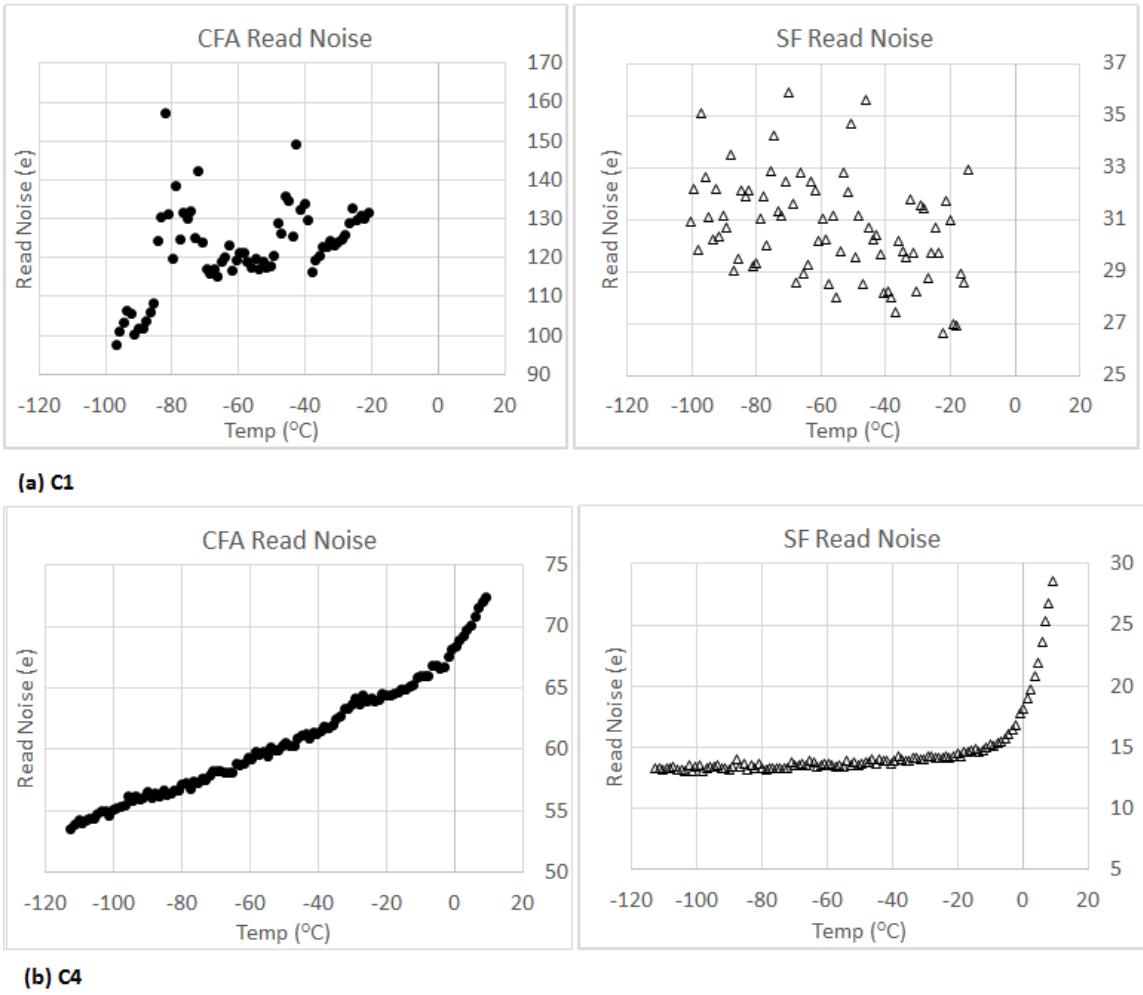


Figure 5.7: Read noise for the (a) C1 and (b) C4 chips.

5.2 Linearity versus Temperature

Unit Conversion and Variance PTC Methods

The linear transfer curves collected in this test are initially a plot of output signal in DN (S_{DN}) vs. number of LED flashes (f_{LED}). These values need to be converted into absolute values of output voltage (V_{out}) vs. charges per packet (N_q) for comparison to the preliminary data collected by Lincoln Labs (Fig. 3.4). S_{DN} is converted to V_{out} by using the conversion factor of the ADC in (V/DN). For example, the ADC resolution is 2^{16} DN over a input voltage range of $\pm$10 V so the conversion factor was 20 V / 2^{16} DN. Converting f_{LED} to N_q is a multi-step process that begins by finding the slope of the S_{DN} vs. f_{LED} plot. This slope gives the linear transfer gain K_{LT} in units of (DN/flashes). Next the gain of the camera K in (e^-/DN) is found. The gain K is the slope of the plot of signal variance (σ^2) vs. S_{DN} [10]. This method of finding the gain is called variance PTC. Finally the LED flash count is multiplied by both of these values to result in N_q (Eq. 5.2).

$$f_{LED}(N_{flashes}) \times K_{LT}(\frac{\text{DN}}{N_{flashes}}) \times K(\frac{\text{e}^-}{\text{DN}}) = N_q(\text{e}^-) \tag{5.2}$$

Linearity Measurements

The linear transfer curve of the C1 imager at 11.4°C is plotted in Fig. 5.8. The SF and CFA outputs saturated at approximately 60 ke^- and 140 ke^- respectively, indicating that the CFA was able to store a larger amount of charge than the SF. These values are much lower than the saturation levels of 200 ke^- for the SF and 1 Me^- for the CFA as measured during the preliminary tests at Lincoln Labs (See

Fig. 3.4). The driving voltages used in this study were not set to optimal levels, so it is unlikely that the sense node capacity was at a maximum, which could explain why the SF saturated at only 60 ke$^-$. Lincoln Labs noted that the positive power supply on the op-amp in the CFA probably set the limit of the output [3]. In that test the CFA op-amp had a 25V positive rail and saturated at approximately 20V. The op-amp in this study was powered with a 5V positive rail, which could be one of the reasons that the CFA in this study had a maximum output of approximately 4V. Future work will be directed at optimizing the capacity of the CCD and studying the effect the rails of the op-amp have on the saturation level.

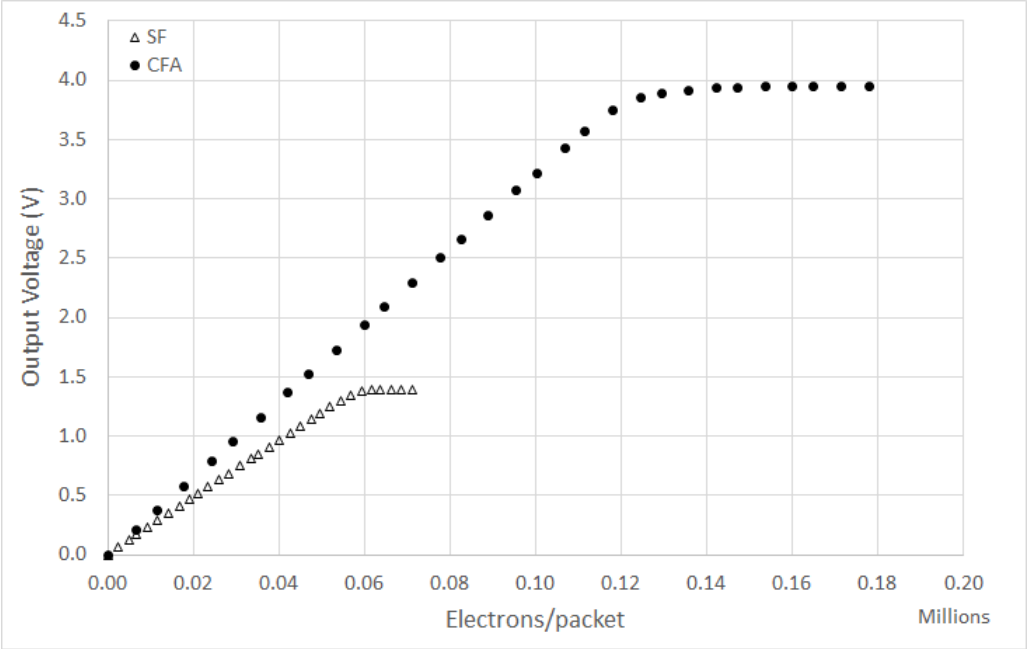


Figure 5.8: Output of the CFA and SF sides of the CCD at a temperature of approximately 11.4°C.

Although the LabVIEW data collection program was eventually designed to only collect data in the linear region and not in the saturation region (See Section 4.5.1), data from this preliminary test is spread over both regions for all temperatures. Before fits of the linear region could be found, the saturation data had to be excluded. This

was done by programming the analysis software to find fits for only the first section of the data up to a certain number of data points. It was necessary to verify that the chosen number of data points would not skew the results of the Linear Residuals (ΔLR) calculations. Therefore the ΔLR vs. temperature data for a single test was plotted multiple times using an increasing number of data points (Fig. 5.9). The number of data points used in the analysis has little effect on the calculations over the temperature range -100°C $< T <$ 10°C. Dark current increases at higher temperatures. This limits the dynamic range, which means that there are fewer data points in the linear region of the linear transfer plots. Figure 5.9(b) shows that calculations using the first 17 data points of the linear transfer curve do not contain saturation data. Therefore the ΔLR analysis was done using the first 17 data points from both the CFA and the SF.

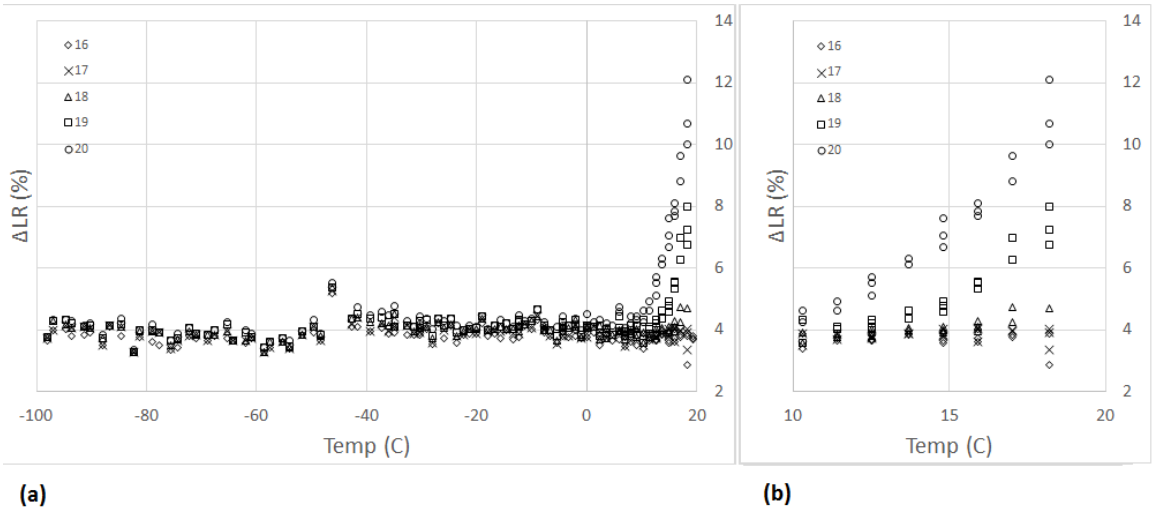


Figure 5.9: (a) Comparison of the ΔLR of the CFA side of the C1 chip for a different number of data points in the linear region of Fig. 5.8. Changing the number of data points used in the analysis does not have a significant effect on ΔLR at low temperatures. (b) An enlargement of plot (a). The effect that data from the saturation region has on the ΔLR can be seen at warmer temperatures.

The ΔLR for the SF and CFA sides of the C1 imager are plotted in Fig. 5.10. The CFA shows a smaller ΔLR than the SF over the entire temperature range. Fur-

thermore, the CFA also exhibits a more stable linearity as the temperature increases, with a standard deviation of nearly half the SF output. While this data does suggest that the CFA output is more stable than the SF, the linearity of both amplifiers is considerably worse than other scientific imagers, many of which are capable of a ΔLR of less than 1% [9]. Linearity can be partially improved in future testing with better EMI shielding to the wires carrying the driving and output voltages as well as with modifications to the circuitry of the camera system. Progress has been made on both of these issues, but has been impacted by the formation of deposits on the imaging region of the chips. More detail will be given on the effect the deposits have had on the images at the end of this section.

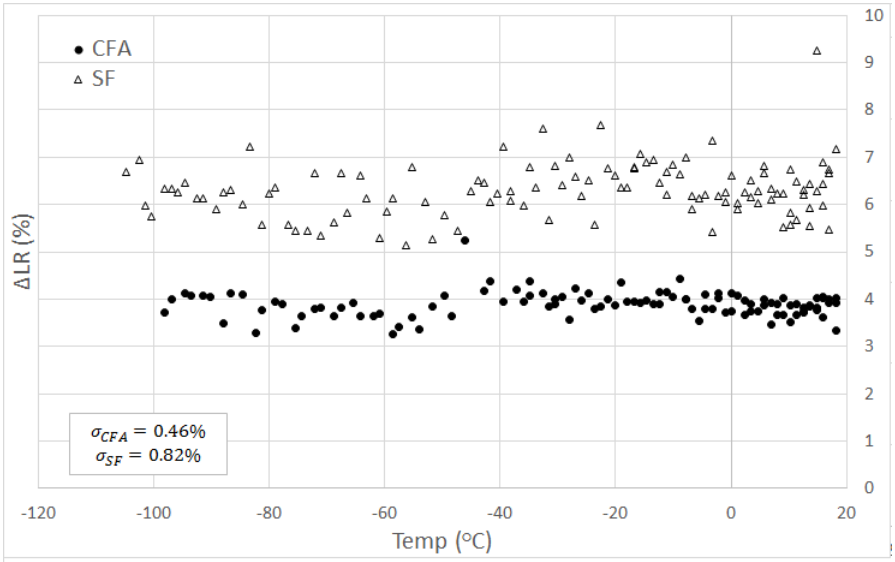
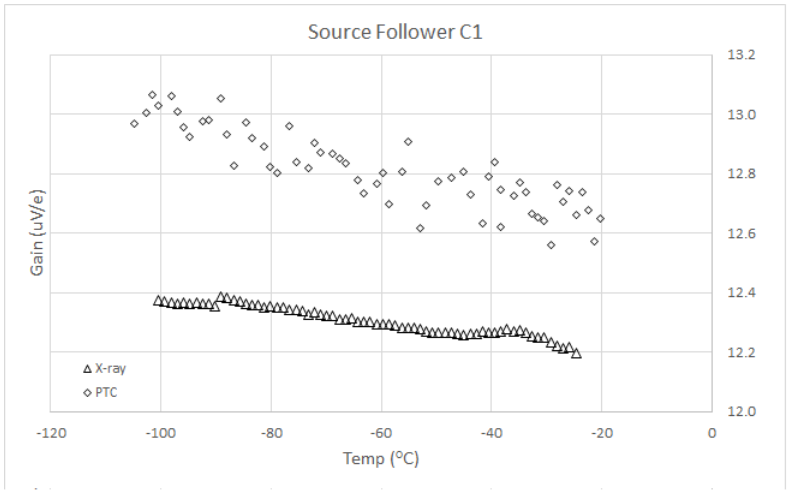


Figure 5.10: Comparison of the ΔLR for the CFA and SF sides of the C1 chip.

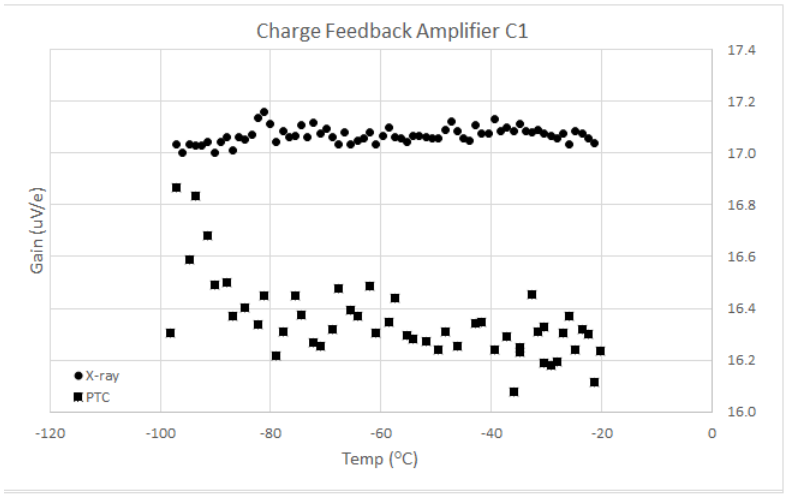
Gain Measurements

The gain of both sides of the C1 imager were calculated using the variance PTC method and compared to the measurements taken using an x-ray source (Fig. 5.5). Plots of these gains are shown in Fig. 5.11. There is a significant discrepancy between

the gains measured in both the CFA and the SF. The x-ray data may be underestimating the gain because the value for η_i may actually lower than the expected 6300 e^- for Cd^{109} due to energy loss to the silicon lattice. This could explain why the PTC data for the SF in Fig. 5.11(a) is greater. However, this would not explain why the CFA gain as calculated by the x-ray source is greater than the gain calculated using the PTC.



(a)



(b)

Figure 5.11: Comparison of the gain of the C1 imager as measured with the variance PTC method and the Cd^{109} source.

It is also interesting to note that the SF output gain is decreasing as the temperature increases for both calculation methods. The variance PTC data was collected using 624 nm red LEDs, which produce no more than one electron per incident photon even at low temperatures. Therefore, the decrease in gain would not be entirely explained as a change in η_i as the silicon pair production energy changes. This suggests that the decrease in gain as measured using the x-ray source could be the result of multiple, undetermined processes.

The spread in the PTC gain data makes clear comparisons difficult. Future work should be directed at improving the resolution of the PTC gain measurements using procedures described by Janesick [9, 10]. Furthermore, gain measurements should be performed using both methods during the same test, so that no variation in gain is expected and a clear comparison can be made.

Read Noise

Read noise in e^- could not be plotted as it was in Fig. 5.7 because reliably accurate x-ray gain data was not taken during the linearity tests. Table 5.2 lists the average read noise for both sides of the imager from the same data set used to plot Fig. 5.10. The gain is estimated using the variance PTC method as described above. The CFA shows better linearity despite having a higher read noise. This suggests that an amplifier's read noise may not be the most important variable in linearity.

Output	$\bar{\sigma}_{read}$ (DN)	K (e^-/DN)	$\bar{\sigma}_{read}$ (e^-)
CFA	9.7	9.5	92.2
SF	4.6	12.8	58.9

Table 5.2: Average read noise of both amplifiers during the linearity test.

Deposits

The results of the linearity tests were affected by the presence of deposits that formed on the surfaces of both chips. It is possible that the source of the deposits is the vacuum grease used on the gaskets of the vacuum chamber, but that can not be verified until every gasket in the vacuum is system is cleaned and a more suitable grease is applied. These deposits created a non-uniform pattern that compromised the flat field illumination created by the LED light box. Early tests showed signs of deposits, but the non-uniform pattern did not appear to have a significant effect on the noise in the imaging region. Figure 5.12 shows an image from the test of the CFA used to plot the ΔLR in Fig. 5.10.

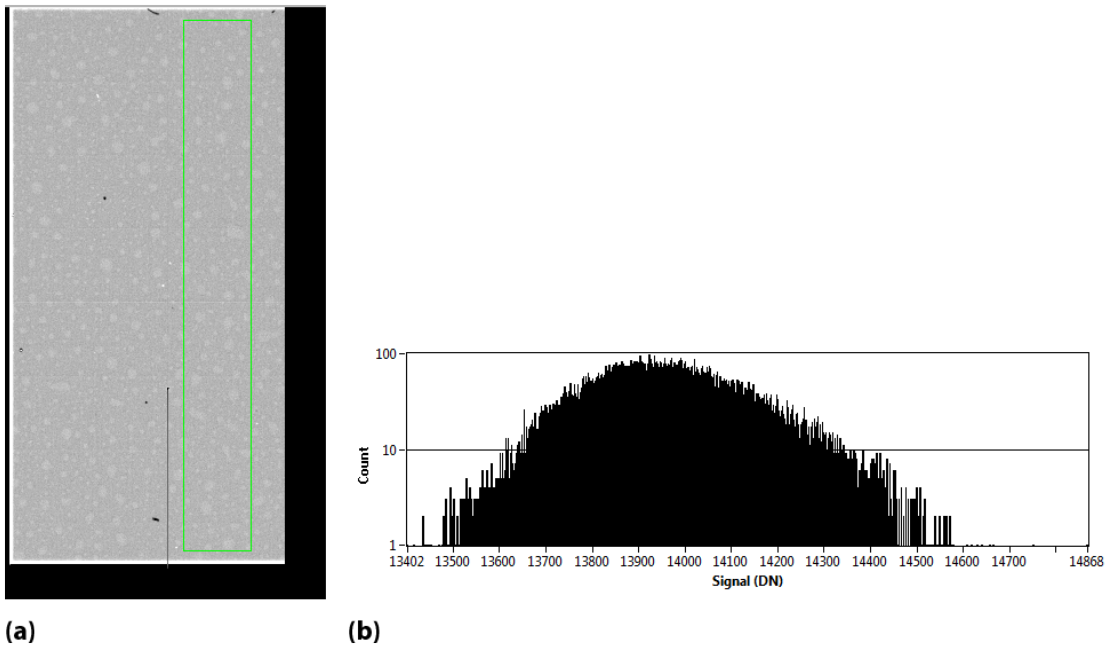


Figure 5.12: (a) Image from the data set used in Fig. 5.10. The image was taken with the CFA output. The dots spread across the image are caused by deposits on the surface of the chip that partially absorb light from the LED light box. (b) Histogram of the boxed region in (a).

The deposits grew in area after multiple tests. Figure 5.13 shows an image from

a more recent linearity test. The deposits have significantly altered the flat field illumination of the chip. This has compromised the linearity of both imagers. Both amplifiers show a greatly increased ΔLR (Fig. 5.14). Little difference can be seen in the ΔLR of the SF and CFA outputs. This is because the deposits spread across both sides of the chip and the noise caused by the deposits is much higher in magnitude then the noise from the amplifiers themselves.

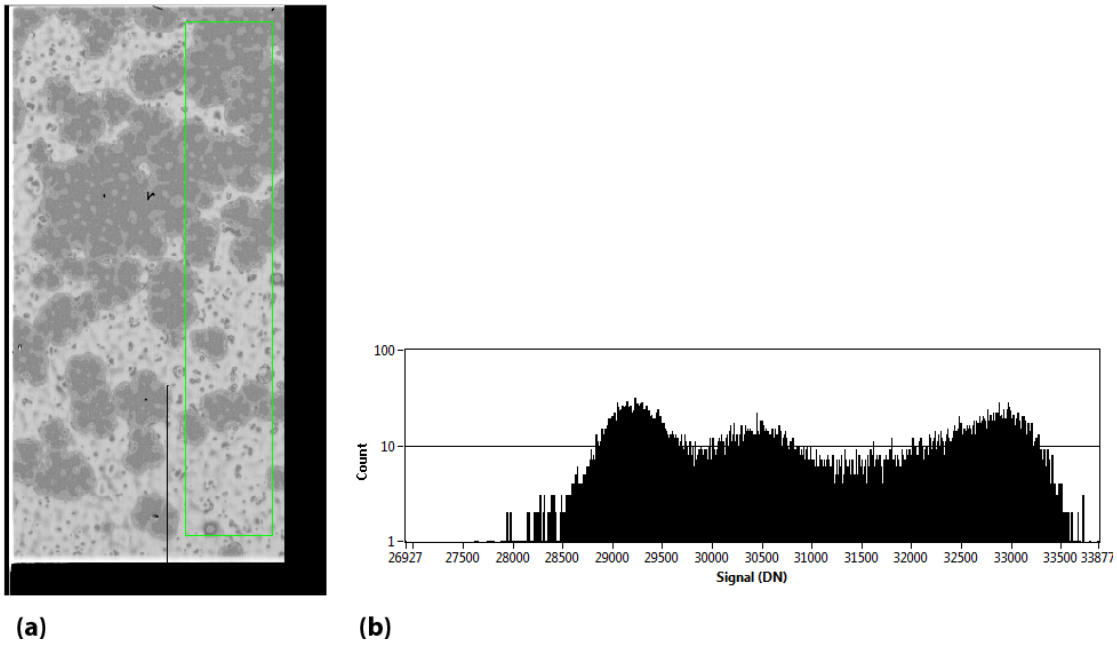


Figure 5.13: (a) Image taken with the CFA side of the CCD showing the effect of the deposits. (b) Histogram of the boxed region in (a).

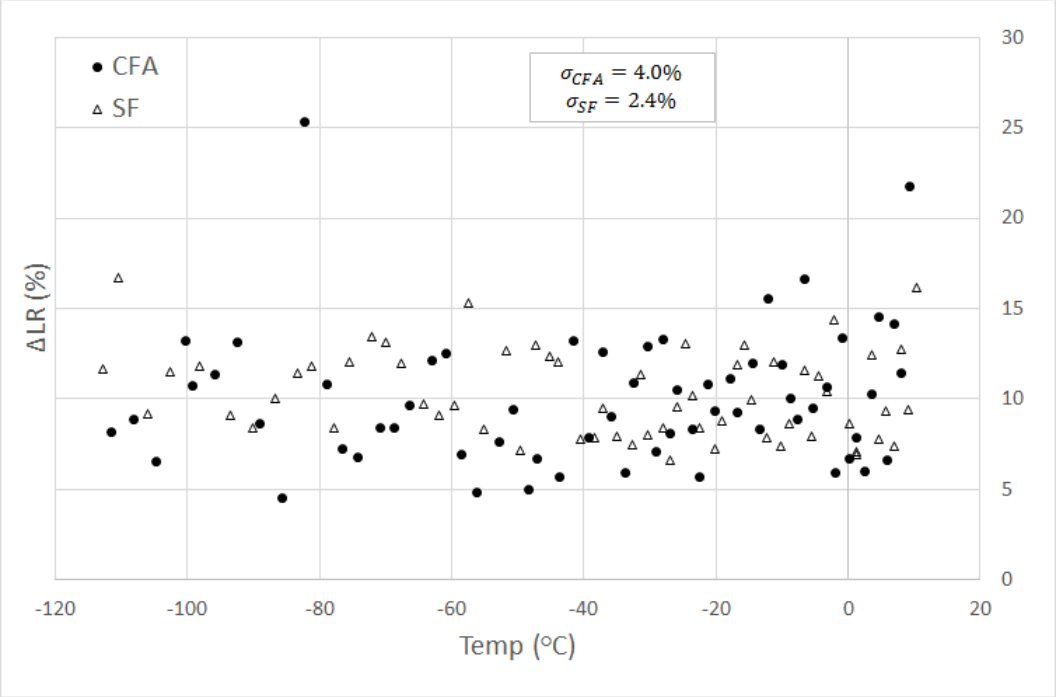


Figure 5.14: Comparison of the ΔLR for the CFA and SF sides of the imager after the deposits grew in area. The deposits on the surface of the imager have significantly altered the linearity of the devices.

Although the average area of the deposits grew after multiple tests, they showed a great deal of variation within a single test as the temperature of the imager increased (Fig. 5.15). Comparing the plot of image noise to the images themselves shows that as the deposits worsen, the noise of the imaging region increases.

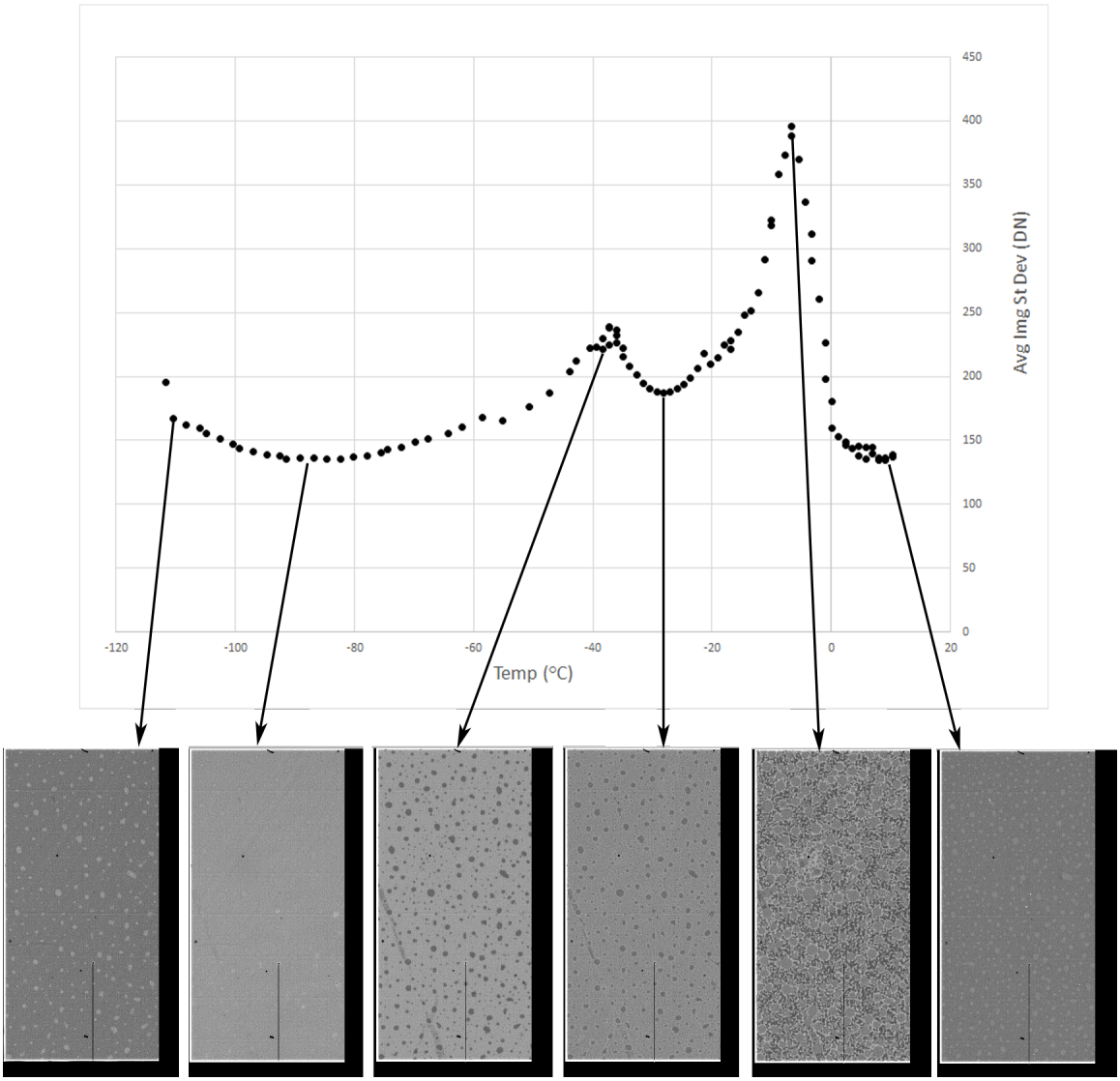


Figure 5.15: Images from the CFA side of the CCD, which show how the pattern of the deposits changed as the temperature increased. Comparing the images to the graph of the standard deviation of the imaging area show that the deposits have an affect on the image noise.

It was found that the deposits could be avoided by using only a scroll pump rather than a turbo pump. Apparently either the turbo pump is the source of contamination or a substance is vaporizing at low pressure. By using only the scroll pump and not the turbo pump, the minimum pressure inside the vacuum chamber is approximately 10^{-3} torr. Tests have shown that this is sufficient to eliminate the risk of damage

due to condensation. The chips have been returned to Lincoln Labs for cleaning and future linearity tests should not be affected by deposits.

Temperature Variation

The temperature of the CCD was increasing during each linear transfer curve (See Fig. 4.4). It took about three minutes to collect the data needed to produce a single linear transfer curve such as Fig. 5.10. Because of this, some of linear transfers contain data that was collected at slightly different temperatures. The histogram in Fig. 5.16 plots the change in recorded temperature per transfer curve. For example, the temperature of the CCD increased by 1.1°C during 24 of the linear transfer tests. It is not expected that this significantly changed the results of the linear residuals tests, but future experiments could be designed to decrease the duration of data collection by using an analysis method called shutterless photon transfer [9]. In this process, a single unfocused spot of light is incident on the imager, which is continuously read out. The intensity of the spot of light is adjusted to just above the full well of the CCD so that the full dynamic range of the imager is measured in a single frame.

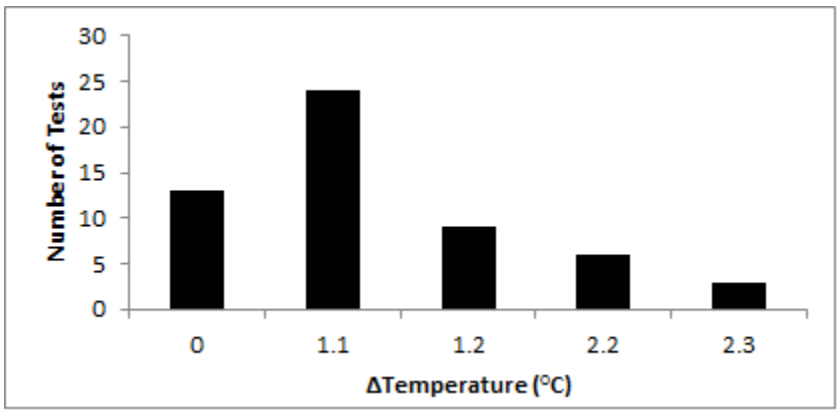


Figure 5.16: Change in CCD temperature during a single linear transfer curve.

6.0 Conclusion

The stability of a CCD is partially dependent on the noise associated with the output amplifier. The sensitivity of the traditional SF amplifier is dependent on the all of the capacitances associated with the reset and output transistors. However, the CFA sensitivity is only dependent on the feedback capacitance. Preliminary analysis of the two output amplifier structures indicates the the CFA may have a number of advantages over the traditional SF because of this. Linear residual curves of the CFA show a smaller nonlinearity over the dynamic range than the SF. Furthermore, the dynamic range of the CFA is significantly larger than the SF. X-ray measurements show that the CFA gain is more stable over a large temperature range than the SF.

While the preliminary data presented in this study does indicate the superior performance of the CFA, a number of issues should be pursued in future work. Verifying the pair production energy of the silicon substrate as a function of temperature, and therefore the number of electrons generated per photon, should be determined so that the gain of the imager can be accurately measured. Accurate gain measurements will also be useful in linearity testing. Because the gain calculated using the variance PTC lacks precision, the ΔLR data was calculated using the data in DN. Deviations from linearity can be caused by slight changes in the output amplifier sensitivity. If the sensitivity of the amplifier was known to a high precision, the plot of ΔLR vs. temperature could be calculated using the linear transfer in V/e^-. This graph

would account for the slight variations in the amplifier sensitivity and should have an improved ΔLR. This would be useful in determining how large a role the amplifier has on the linearity of the chip. It would be worthwhile in future tests to be able to more precisely measure the gain of the chip using an x-ray source immediately before taking data for a linear residual test.

Sampierto et al. found that the CFA also showed an improved stability against changes in the bias of the output FET and of the detector [15]. Future work should explore the effect these biases have on the performance of SF and CFA outputs on a CCD.

Both amplifiers exhibit a significant level of noise. Read noise could be obscuring amplifier characteristics relevant to this work including performance at higher temperatures ($T > 0°\text{C}$). Future work should focus on reducing noise levels as much as possible. This will require determining the source of the noise, which could be a combination of effects both on and off chip.

In addition to further experimental work, a greater understanding of the operation of the amplifiers is necessary. It should be determined what physical processes lead to noise in both outputs, including what impact the choice of op-amp has on the CFA. Simulation Program with Integrated Circuit Emphasis (SPICE) simulations of both output circuits should be developed and compared with theory and measurements.

The preliminary results of this study indicate that a digital imager with a CFA output structure may out perform the stability and range of the traditional SF output. This could have an impact on the design of future scientific astronomical imaging devices including those used in satellites. However, before conclusive statements can be made, further research must be performed to verify and expand upon the measurements done in this study.

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